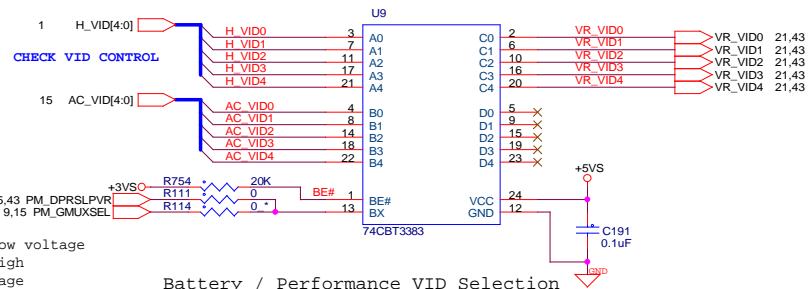


## VID SELECTION



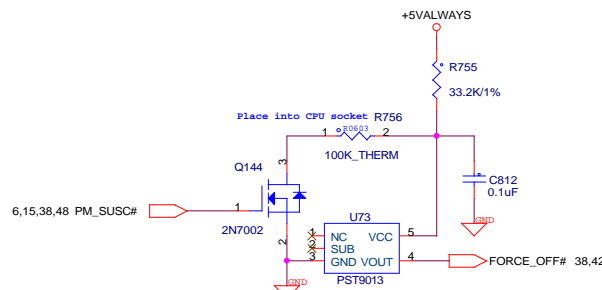
0: low voltage  
1: high voltage

Battery / Performance VID Selection

CBT3383 Bus Exchange

BX	C0-C4	D0-D4
HIGH	B0-B4	A0-A4
LOW	A0-A4	B0-B4

Performance Mode = 1.3V  
Battery Mode = 1.3V  
Deeper Sleep Mode = 1.1V



VID	VCC
4 3 2 1 0	
0 0 0 0 1	1.70
0 0 1 1 1	1.40
0 0 1 0 1	1.50
0 1 0 0 0	1.35
0 1 0 0 1	1.30
0 1 1 0 0	1.15
0 1 1 0 1	1.10
1 0 1 0 1	0.85
1 1 0 1 1	0.70

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**THERMAL & VID Selection**

Size Custom L3C

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XIN\_CLKGEN &  
XOUT\_CLKGEN < 500 mil

May No Stuff:  
Caps are internal  
to clock gen.

Place near receiver.

CLK\_CPUAPIC:  
Should be 2V tolerant.

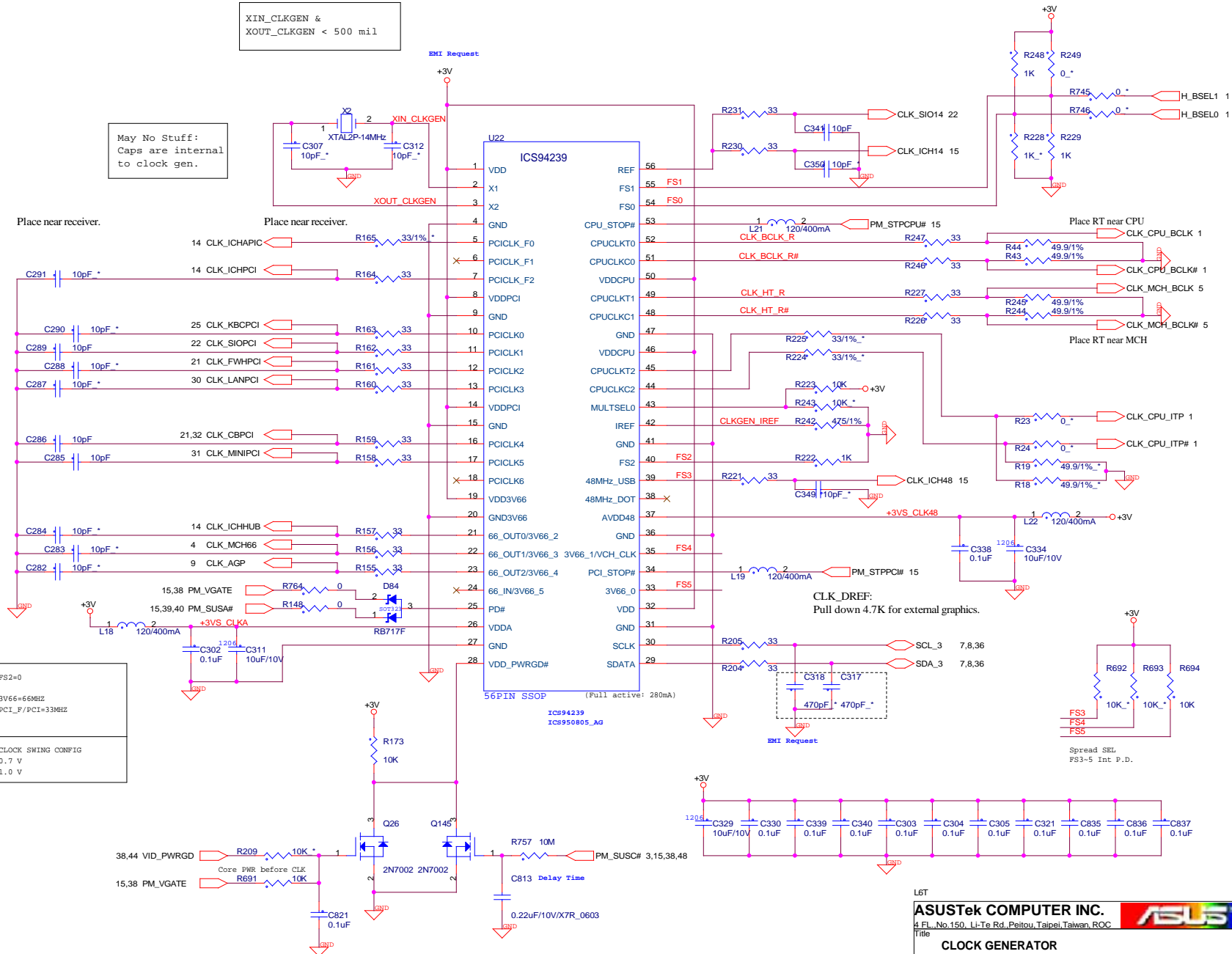
Place all 10pF Caps  
near receiver

For S3 leakage in non-QS stepping

FS1	FS0	CPU	FS2=0
0	0	66.66	3V66=66MHZ
0	1	100	PCI_F/PCI=33MHZ
1	0	200	
1	1	133.33	

MULT0	CLOCK SWING CONFIG
1	0.7 V
0	1.0 V



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CLOCK GENERATOR

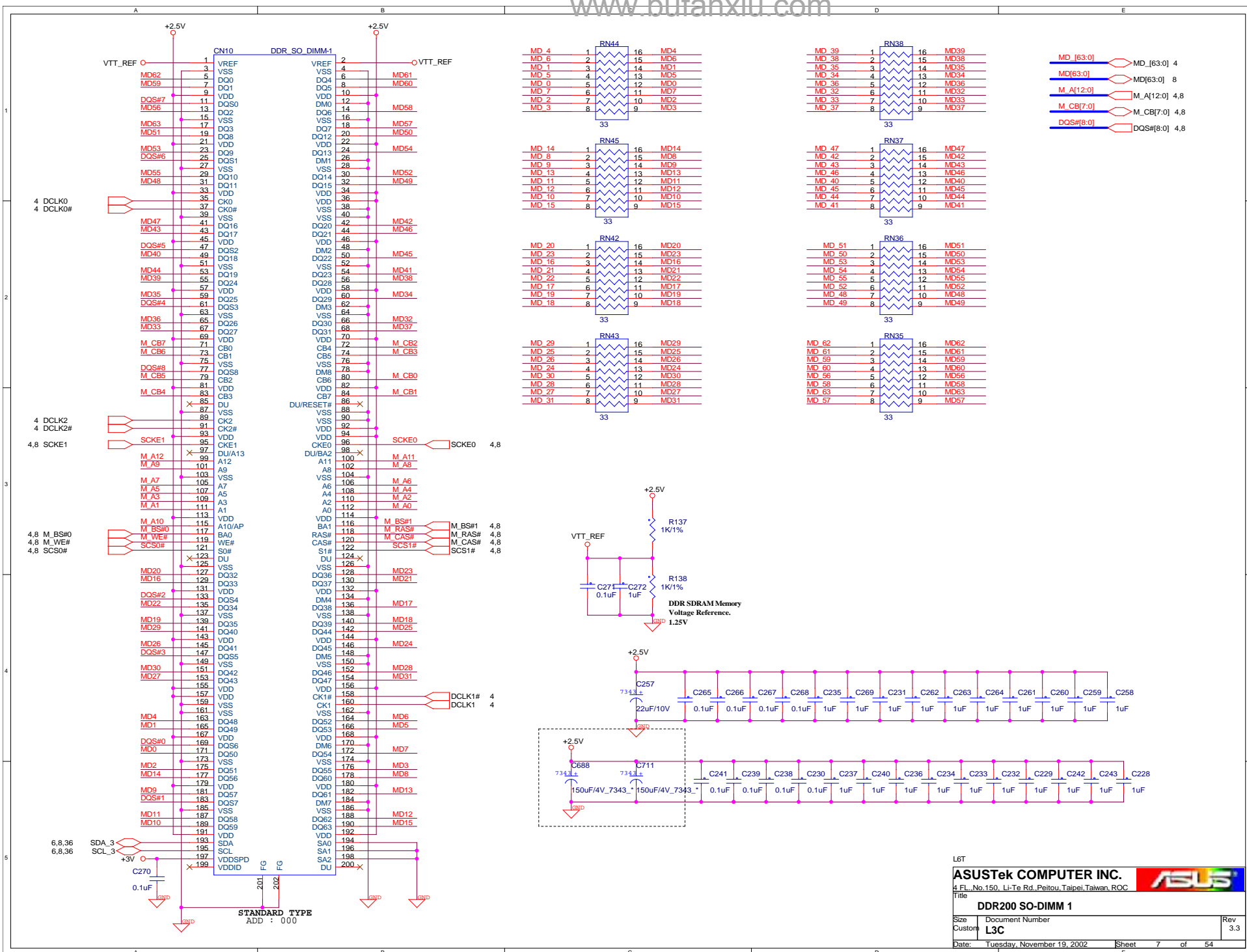
Size Document Number

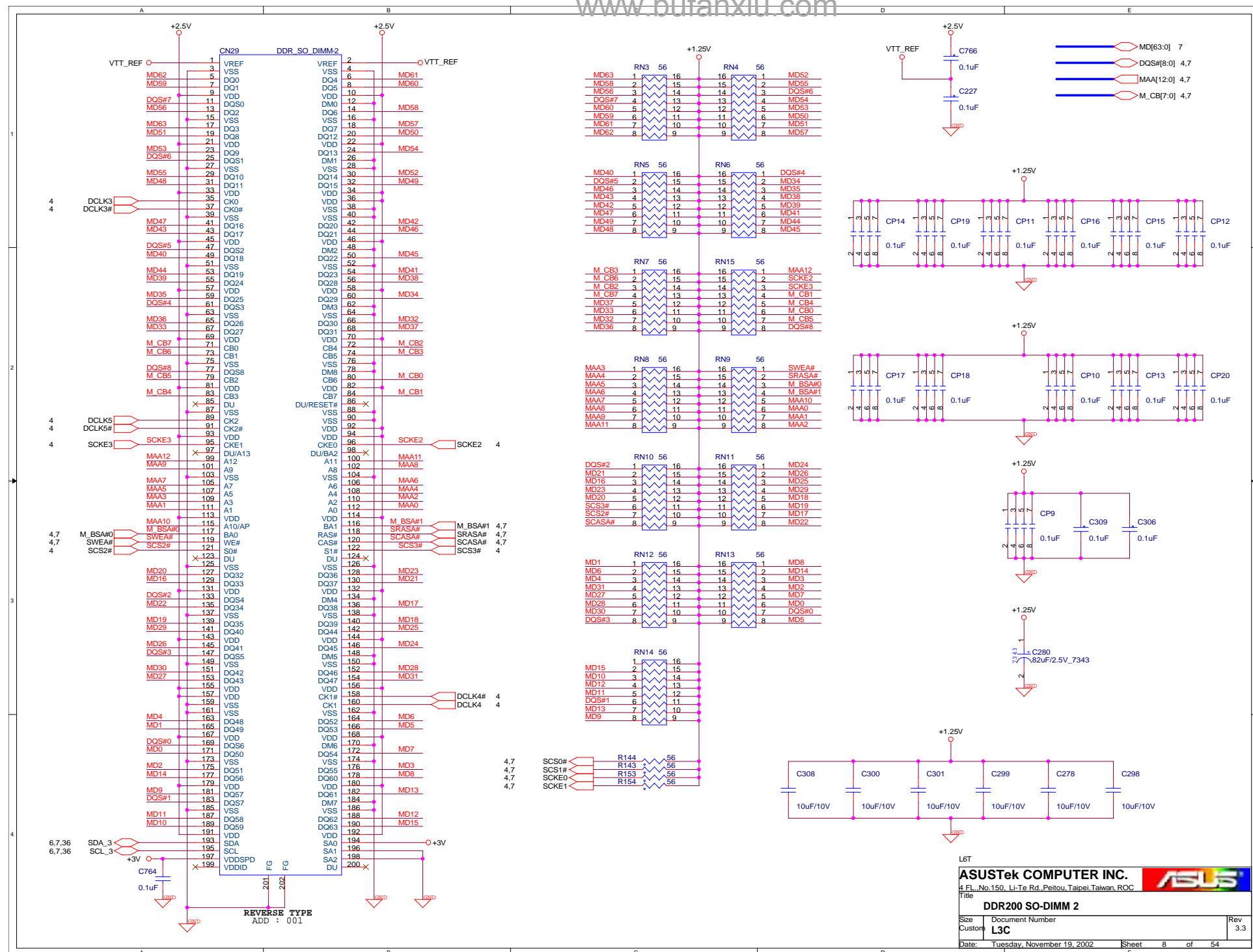
Custom L3C

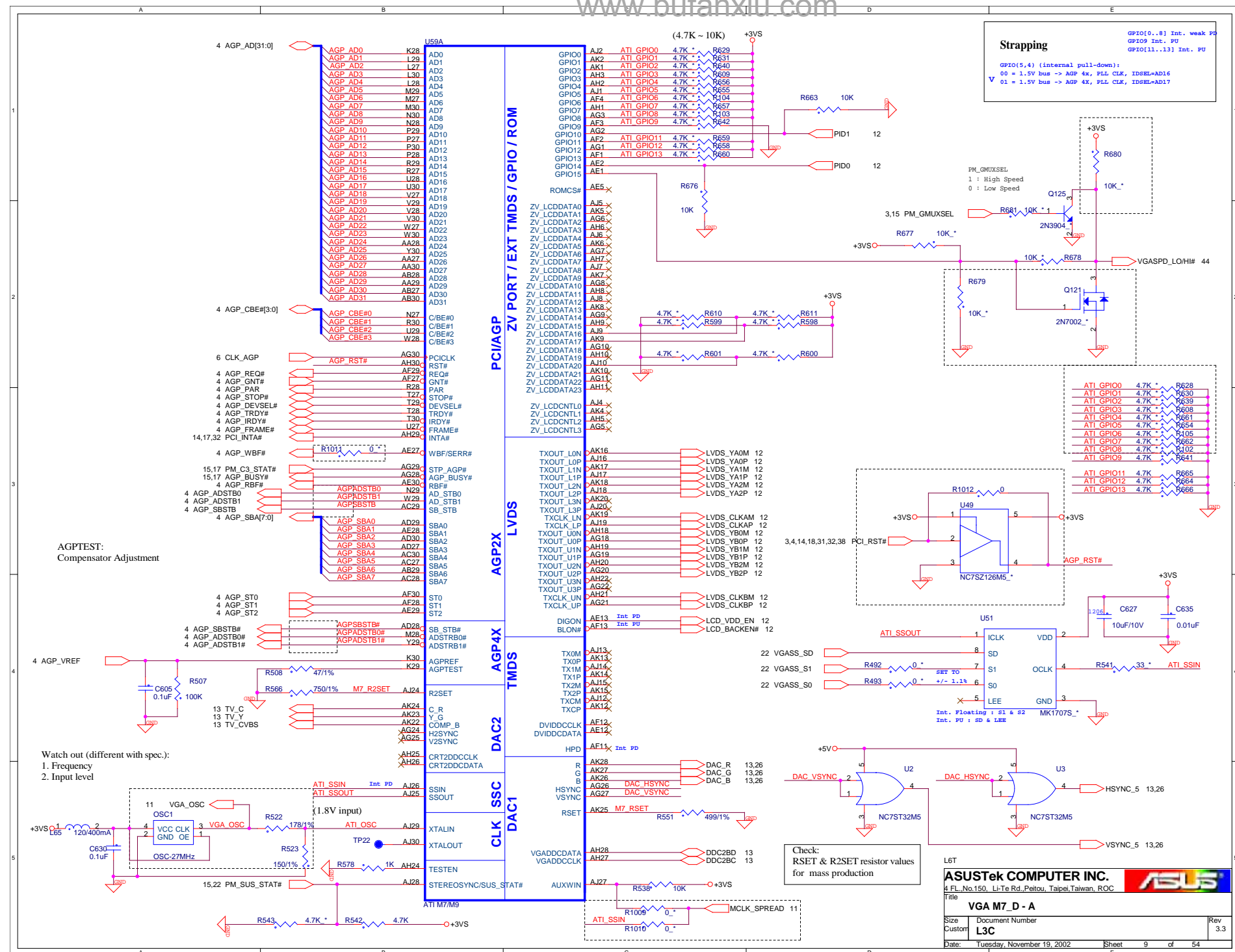
Rev 3.3

Date: Tuesday, November 19, 2002

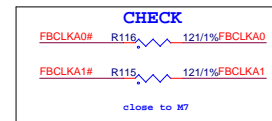
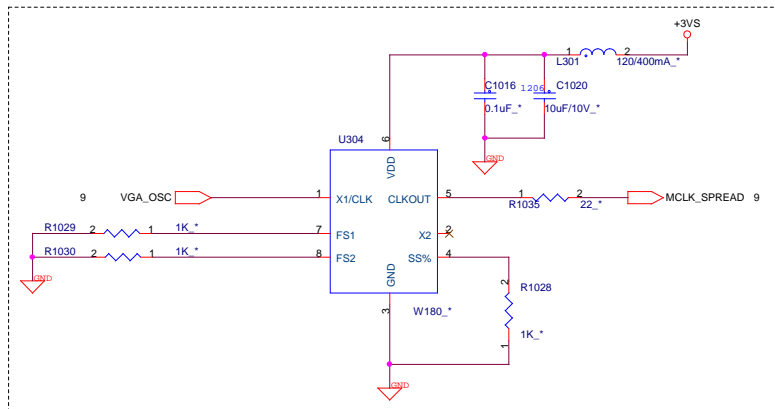
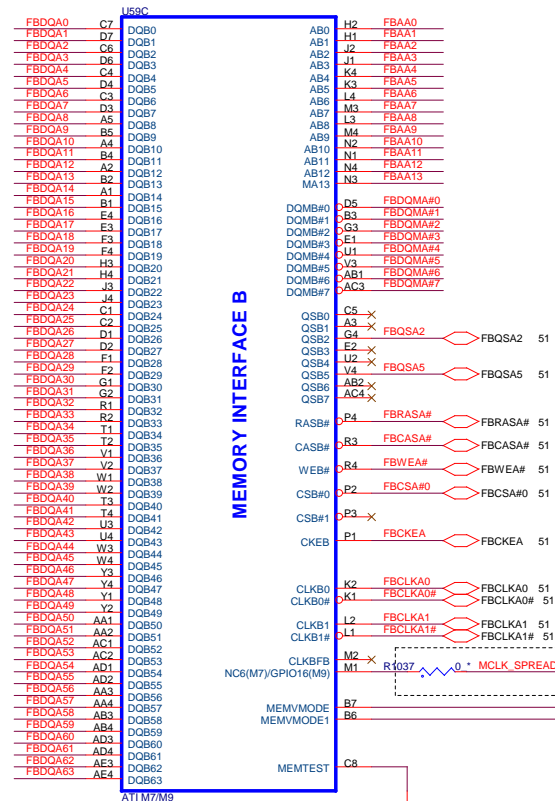
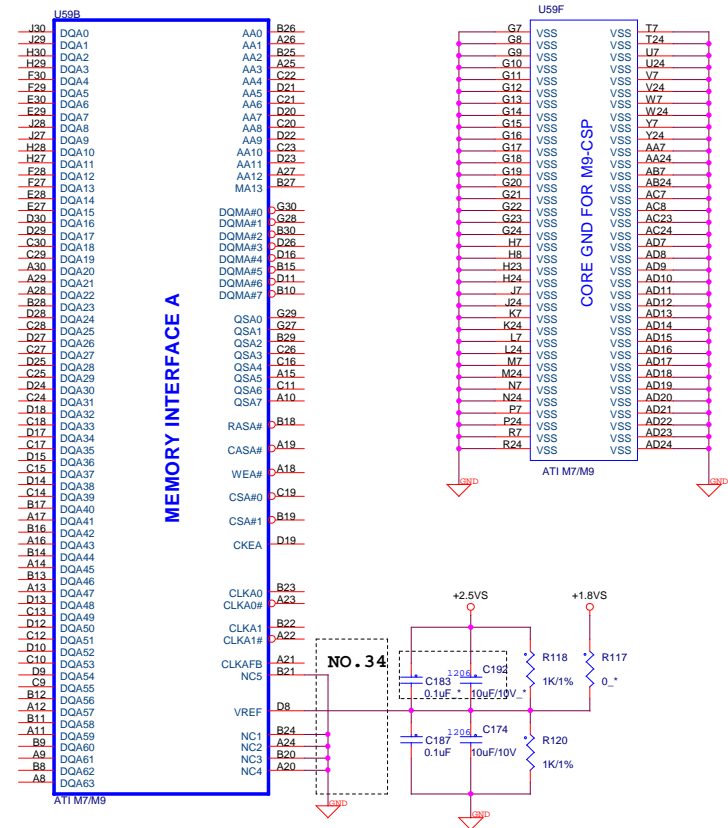
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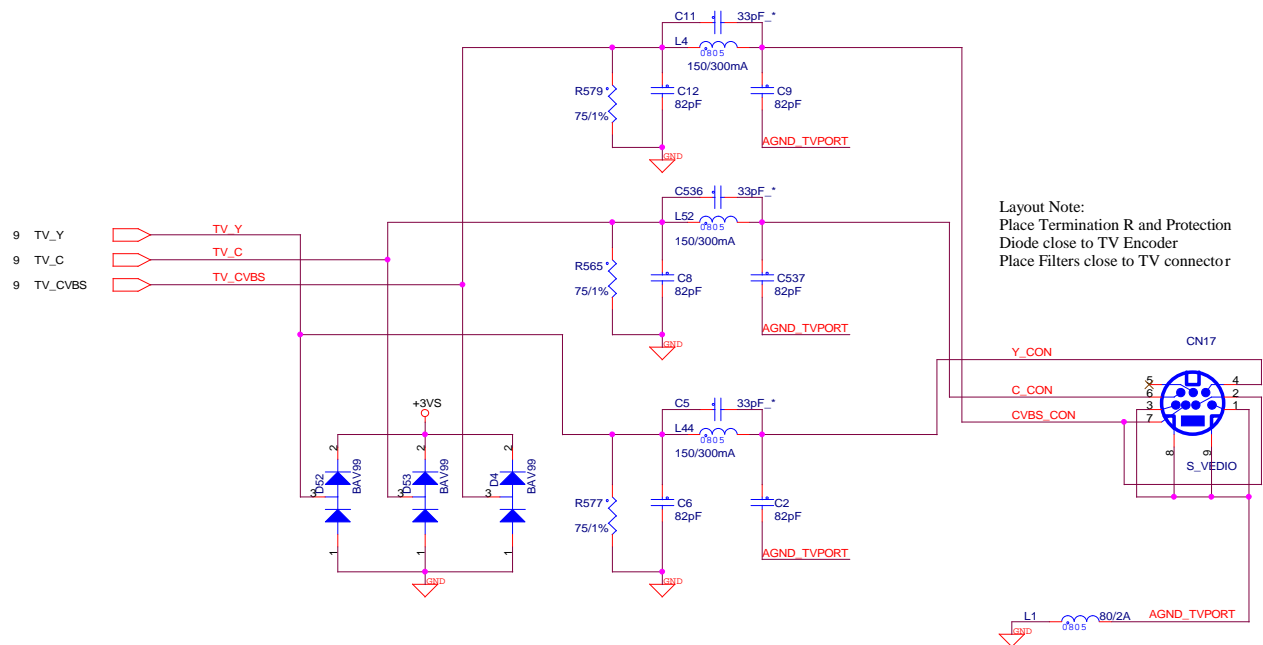
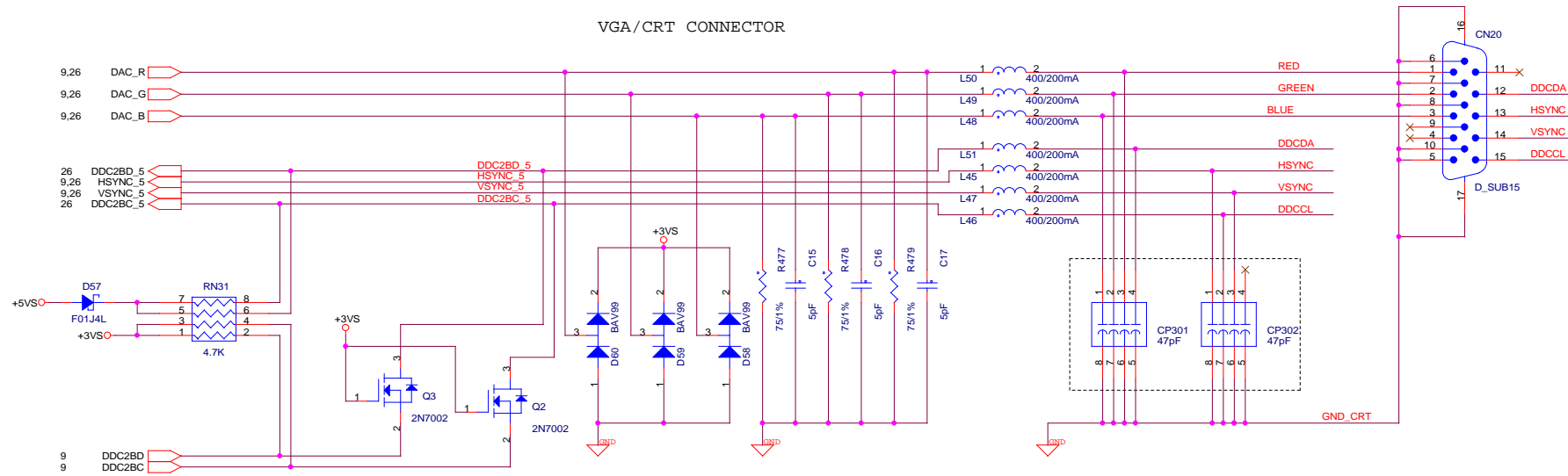
MEMVMODE[1:0]	MEMORY IO VOLTAGE
0 1	2.5V(DDR)
1 0	1.8V(DDR)
1 1	3.3V(SDR)



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Layout:  
ISET -- short and wide trace

## VGA/CRT CONNECTOR



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TV &amp; CRT CONNECTOR

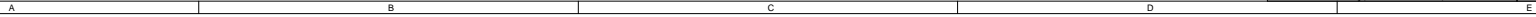
Size Document Number

Custom L3C

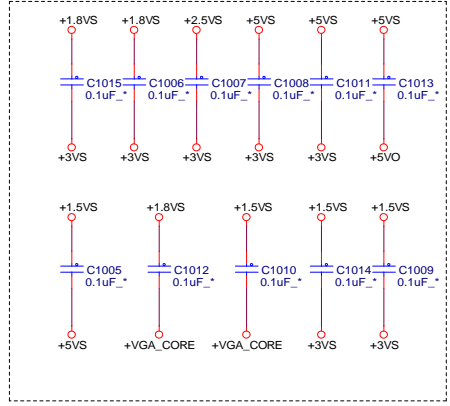
Rev  
3.3

Date: Tuesday, November 19, 2002

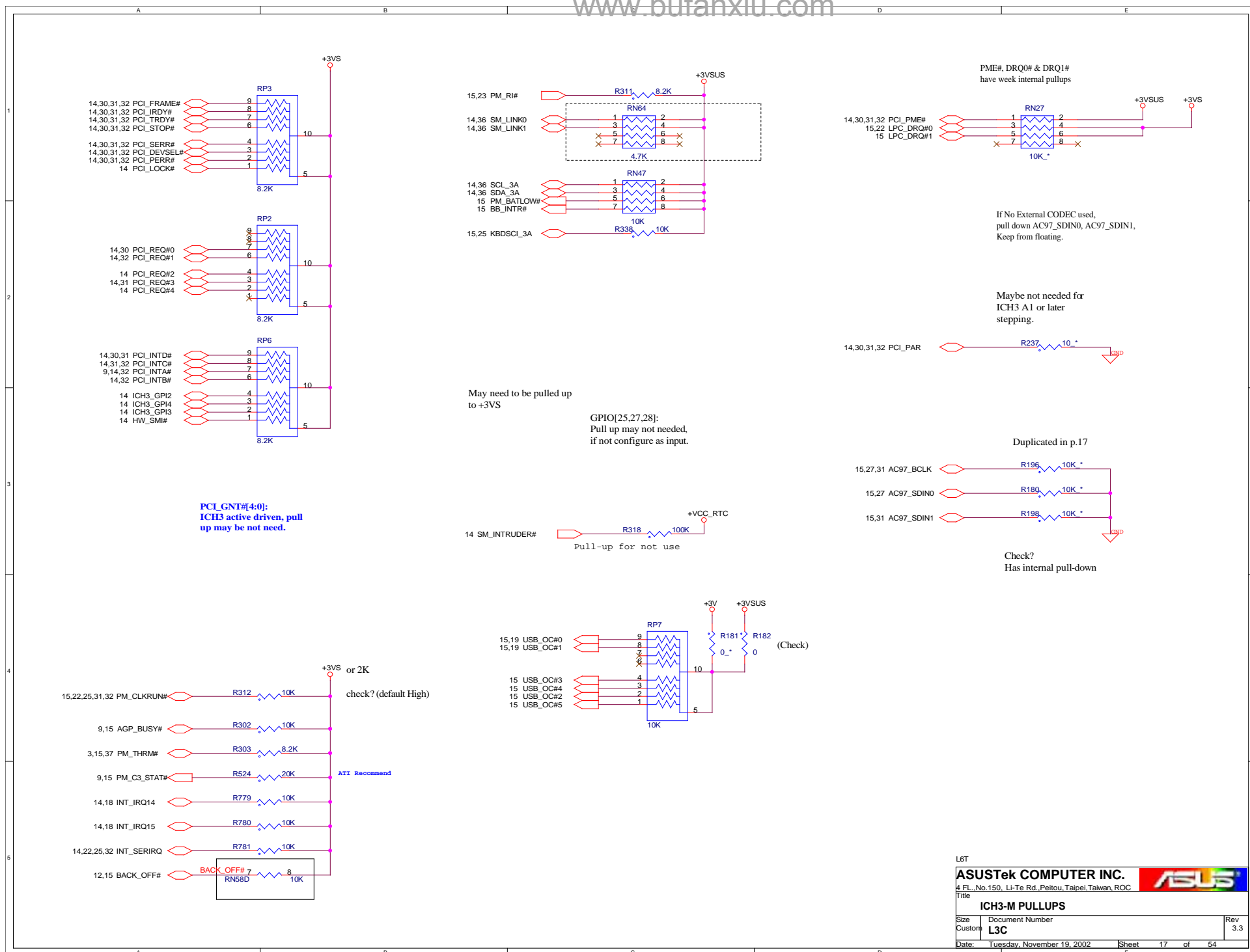
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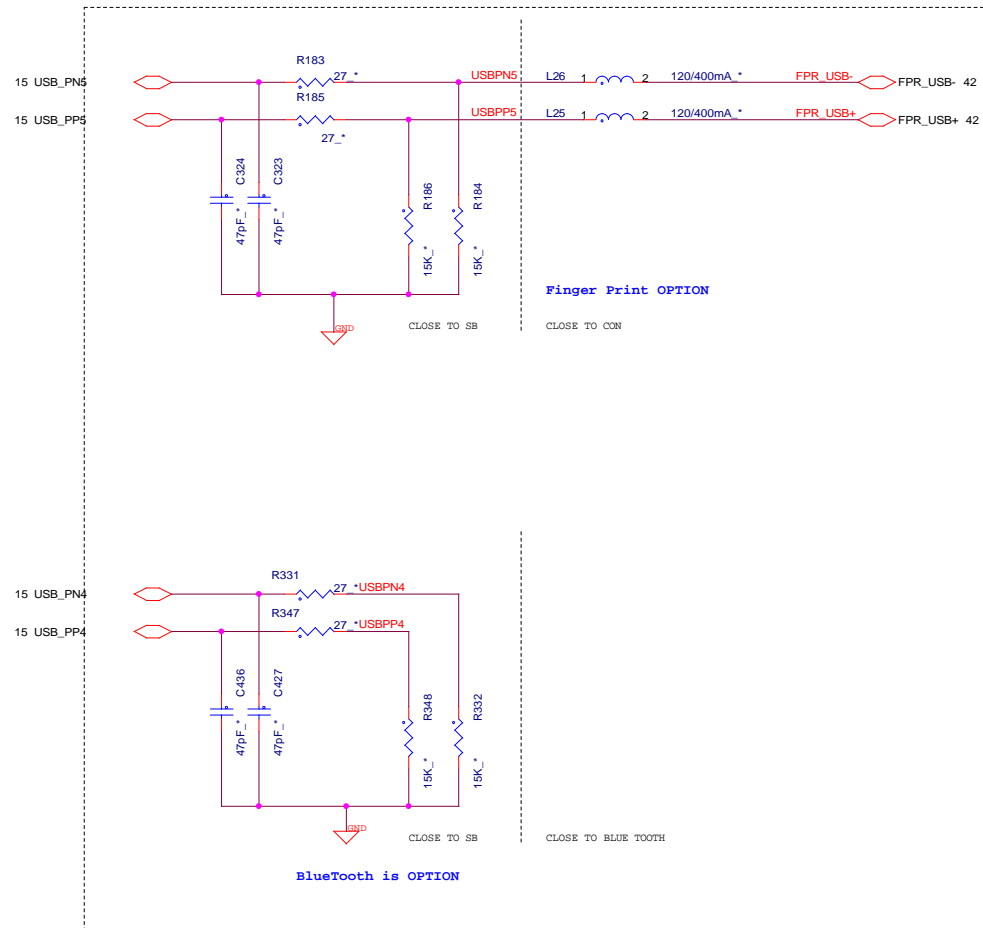
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		E			







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BlueTooth &amp; Finger Print

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Tuesday, November 19, 2002

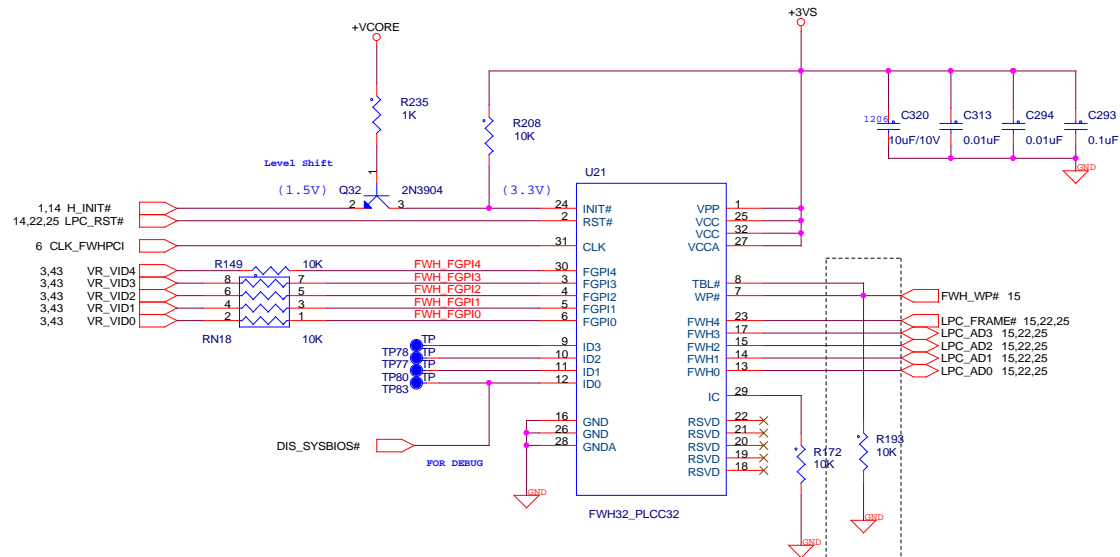
Sheet

20

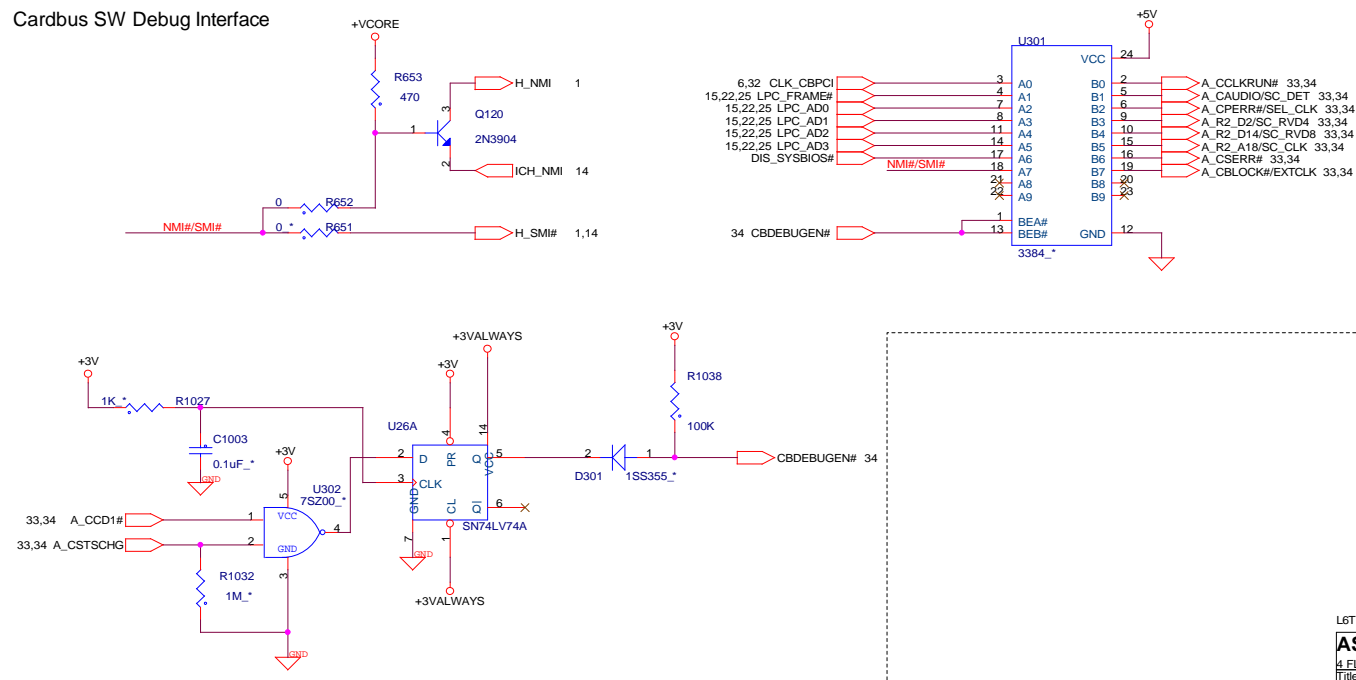
of

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E



## Cardbus SW Debug Interface



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FWH &amp; TEST CONNECTOR

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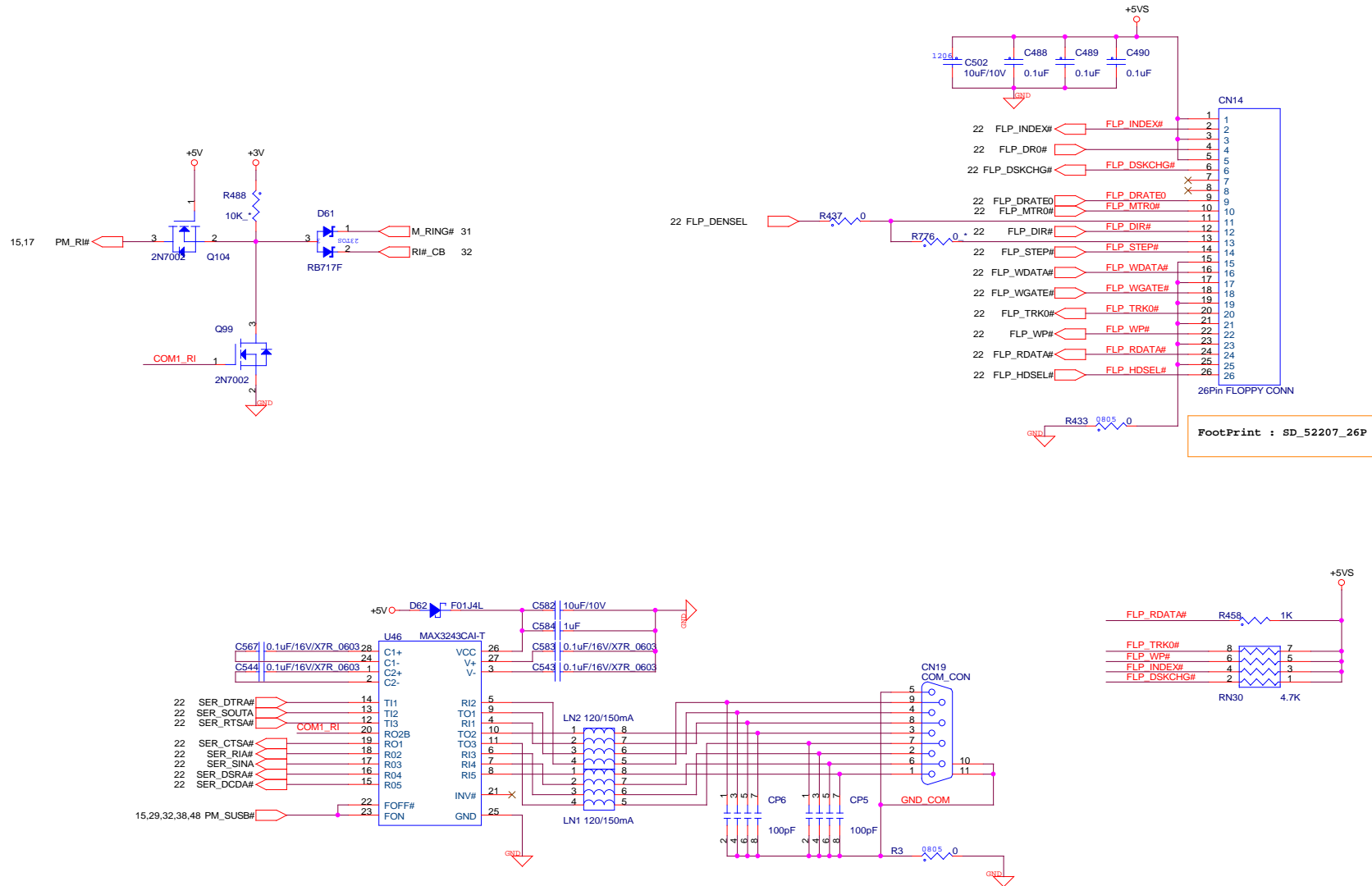
L3C

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COM PORT & FDD

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Date:

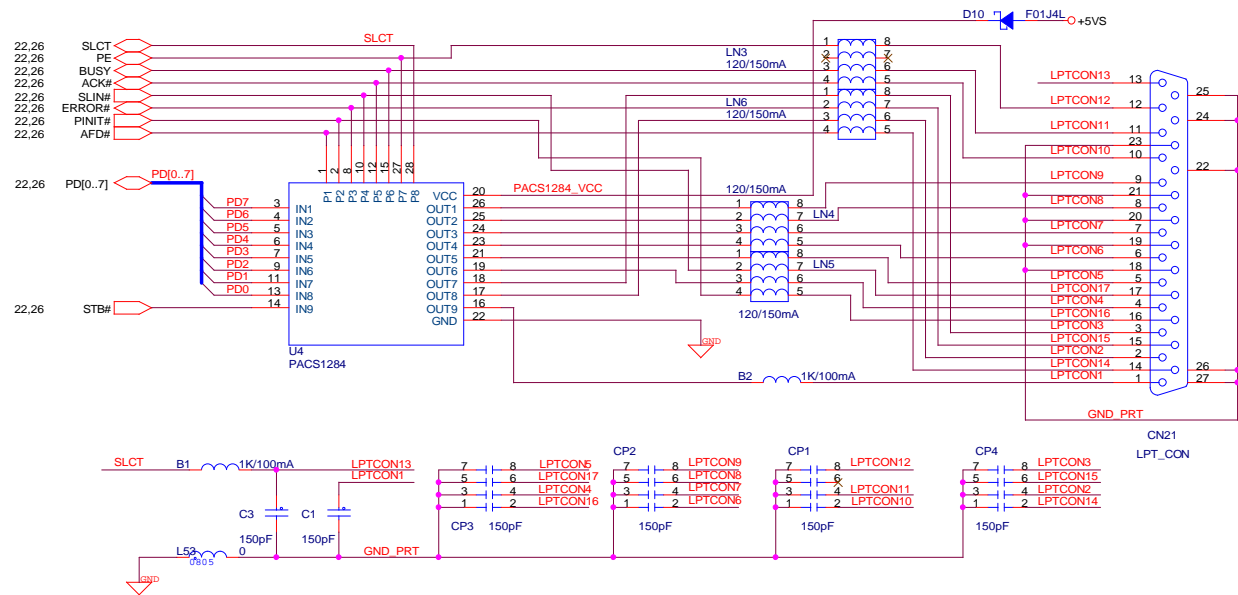
Tuesday, November 19, 2002

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Title	
IR & LPT PORT	
Size	Document Number
Custom	L3C
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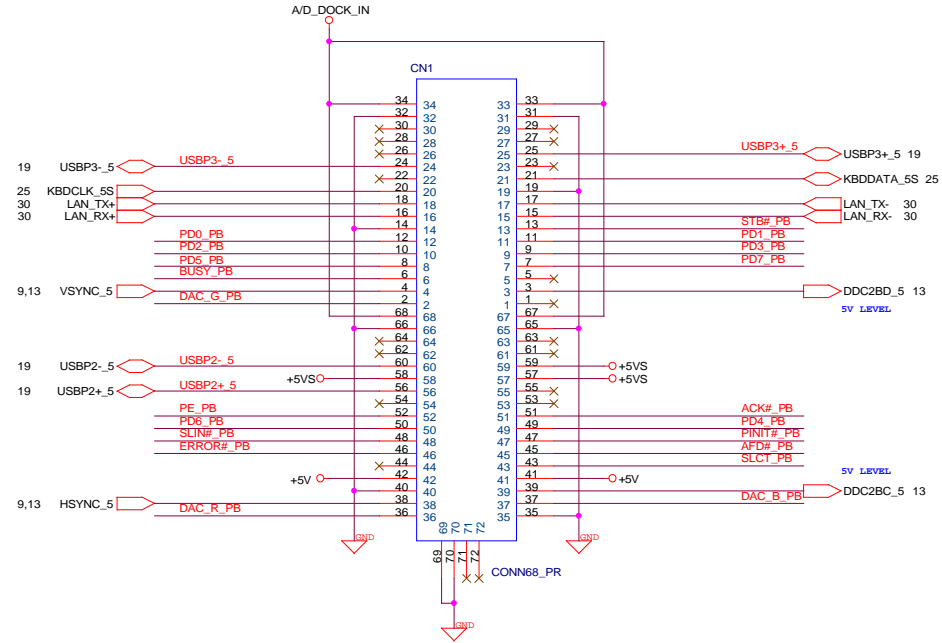


The function difference between Port-DockI / Port Dock II:

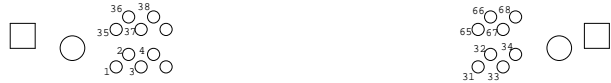
1. PDI w/ COM, 2xPS2, wo/ Lan
2. PDII w/ 2xUSB, Lan, 1xPS2

The Pinout difference between PD1/PD2

1. Remove PD1 Pin:12,13,16-20,30,34,42,59,61-63,68
2. PD1: +19V:35,36,37 / GND:1,2,3,21,38  
PD2: +19V:1,2,35,36 / GND:3,4,16,21,37,38



Top View



22,24 SLCT# SLCT#\_PB  
22,24 PE PE\_PB  
22,24 BUSY BUSY\_PB  
22,24 ACK# ACK#\_PB

22,24 SLIN# SLIN#\_PB  
22,24 ERROR# ERROR#\_PB  
22,24 PINIT# PINIT#\_PB  
22,24 AFD# AFD#\_PB

22,24 PD0 PD0\_PB  
22,24 PD1 PD1\_PB  
22,24 PD2 PD2\_PB  
22,24 PD3 PD3\_PB

22,24 PD4 PD4\_PB  
22,24 PD5 PD5\_PB  
22,24 PD6 PD6\_PB  
22,24 PD7 PD7\_PB  
22,24 STB# STB#\_PB

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PORT BAR II

Size Document Number

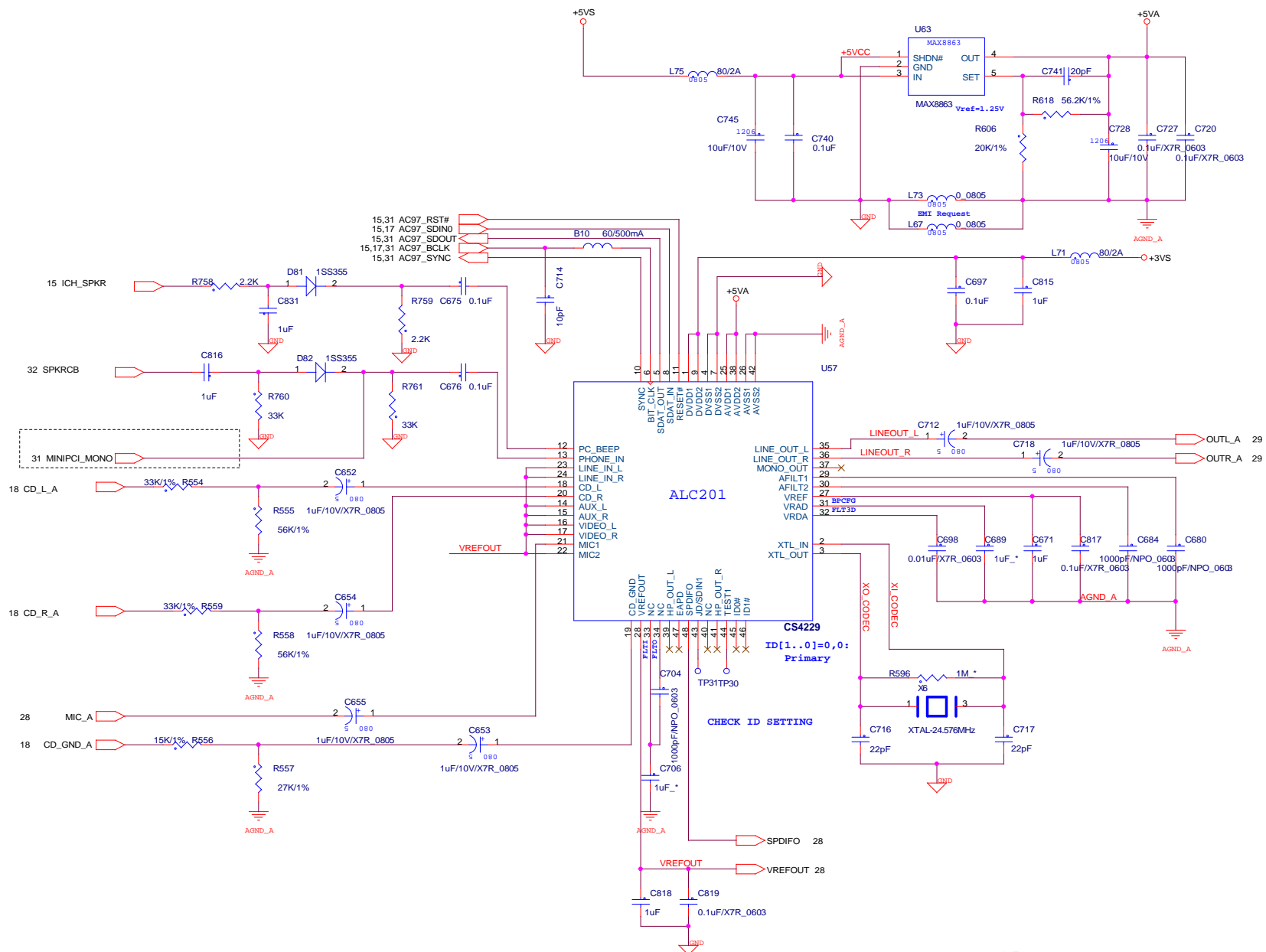
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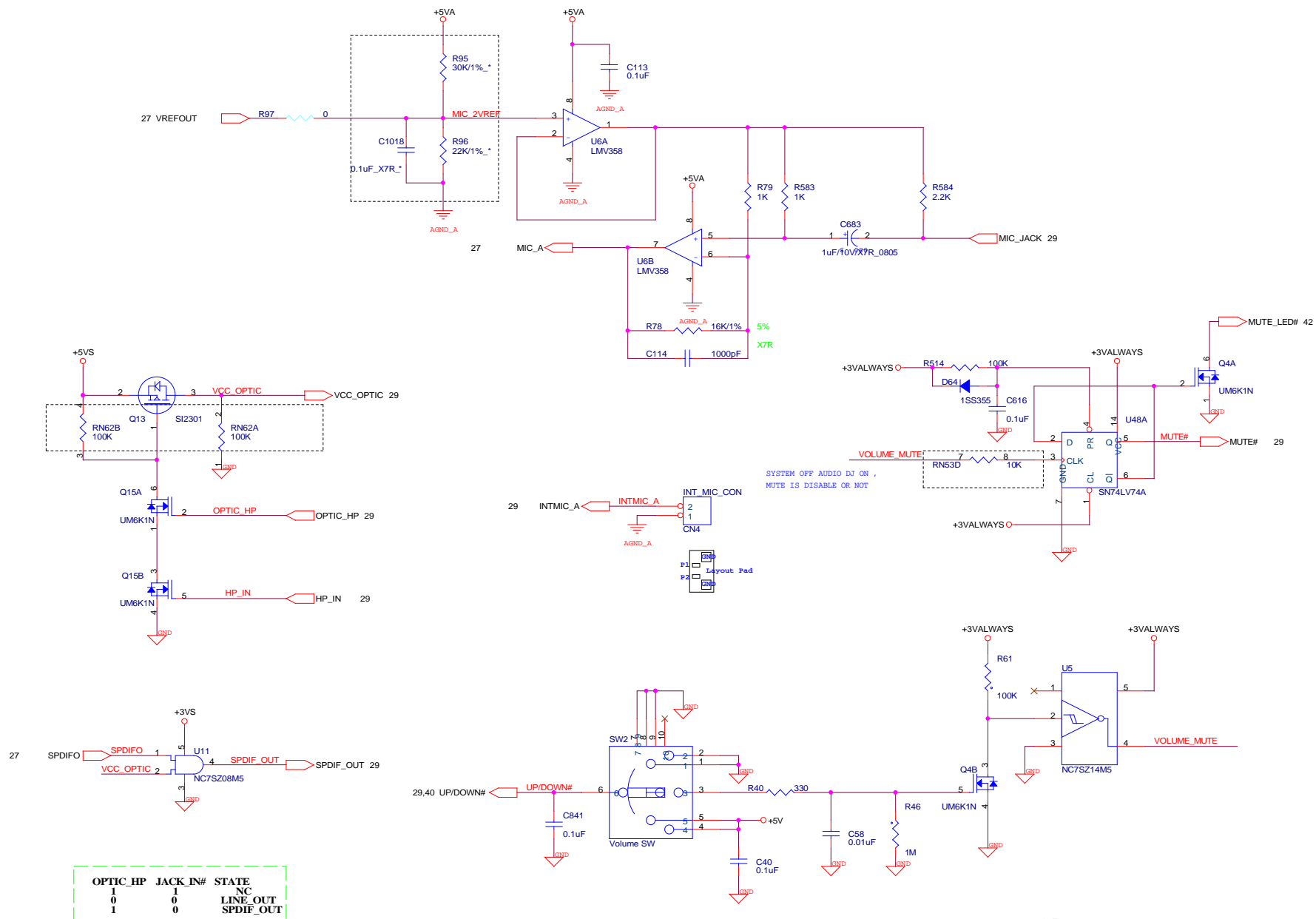
Title

AC97 &amp; MDC

Size  
CustomDocument Number  
L3CRev  
3.3

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Title

MIC AMP. &amp; BEEP GEN.

Size

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Custom

L3C

Rev  
3.3

Date:

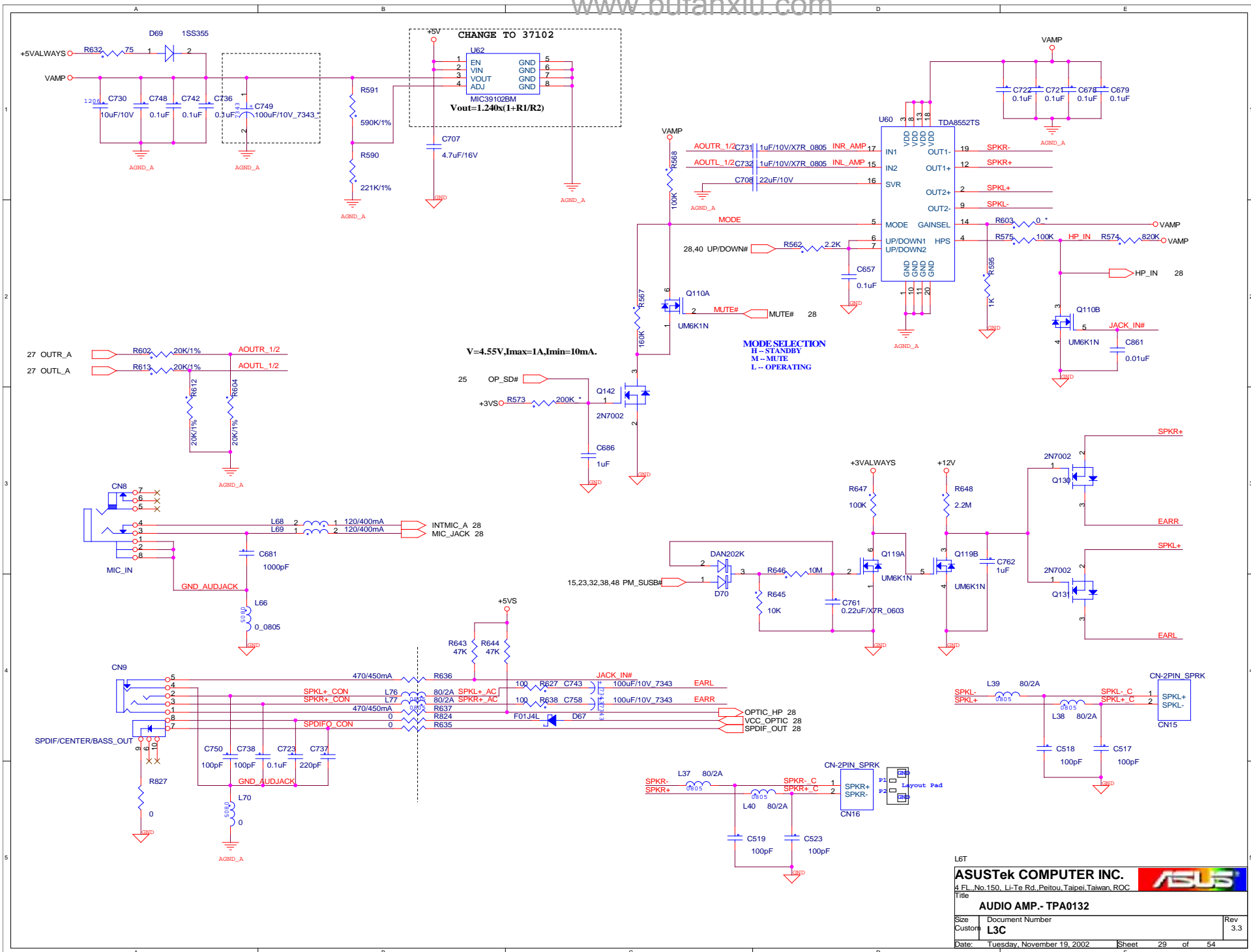
Tuesday, November 19, 2002

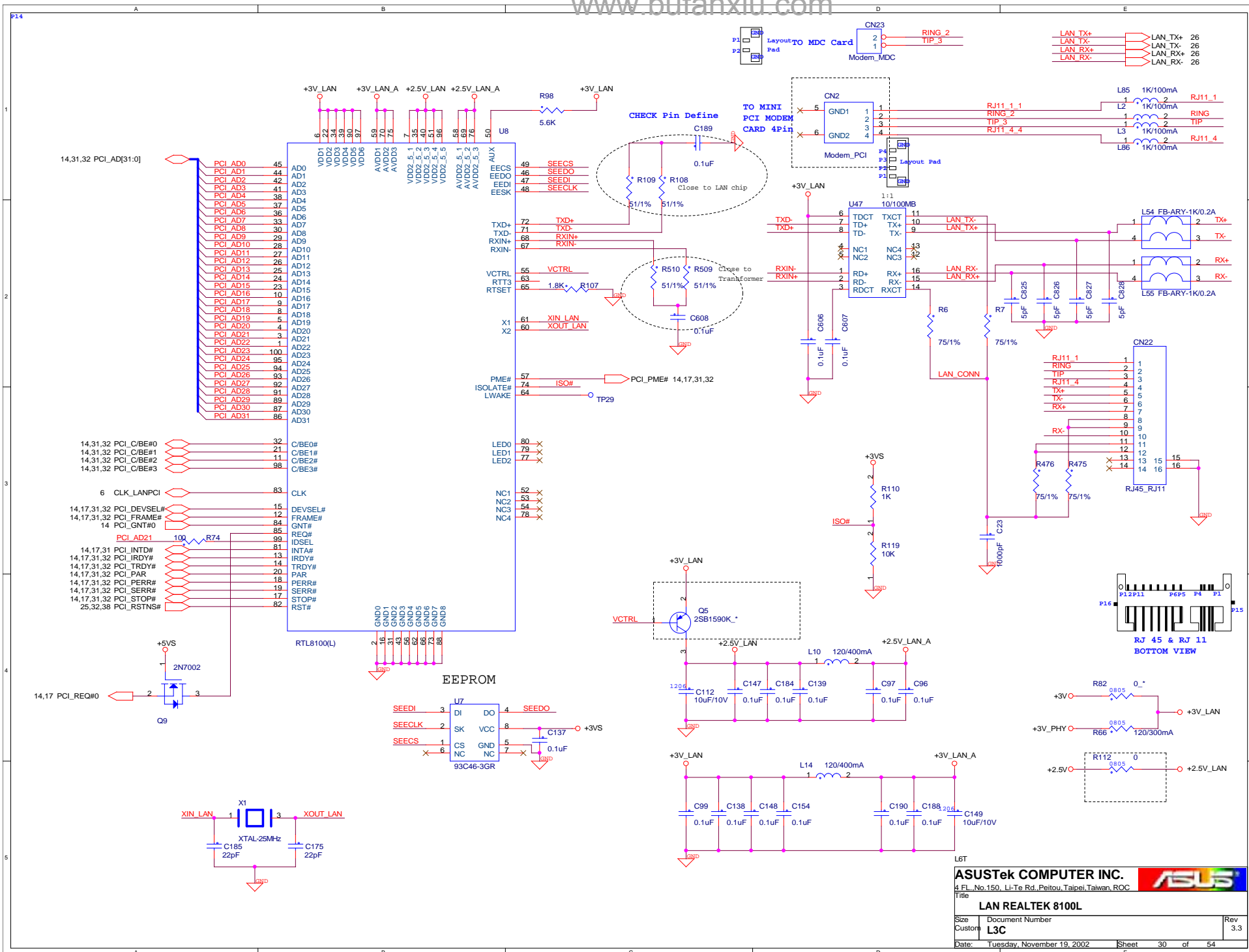
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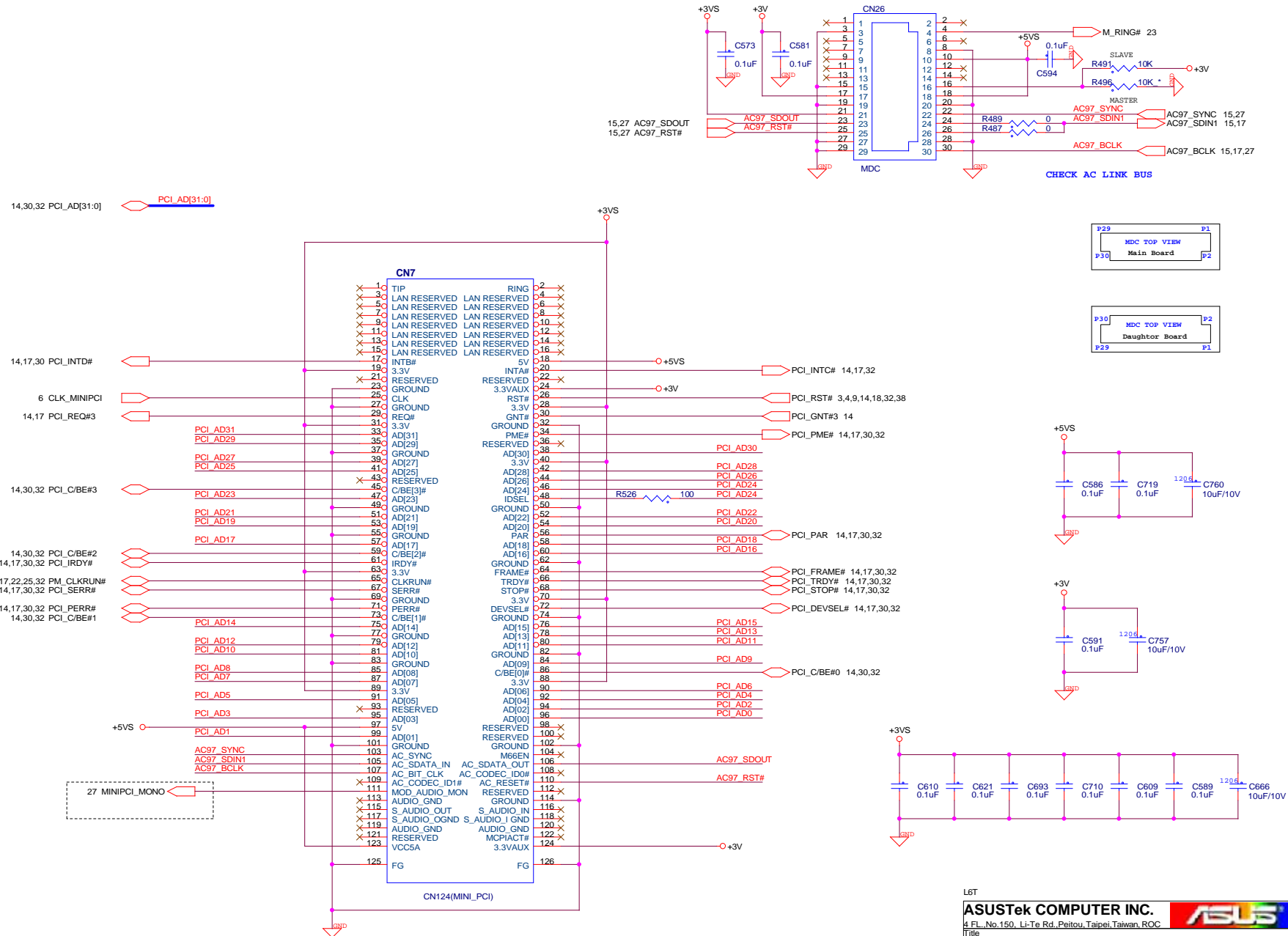
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Title

Mini-PCI &amp; MDC

Size

Document Number

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Rev

3.3

Date:

Tuesday, November 19, 2002

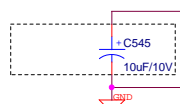
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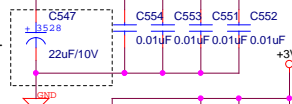
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\*Layout as close as possible to VCCPCI pins.



\*Layout ACAP to VCCCORE pins.



\*Layout ACAP to VCCAUX pins.

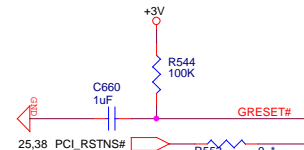


PCI Bus

14,30,31 PCL\_AD[31:0]

#### PowerOnReset for VccCore

\*An option is available that GBRESET# is wired directly to PCIRST# when not using "wake up from D3" power-management scheme.



PCI Bus

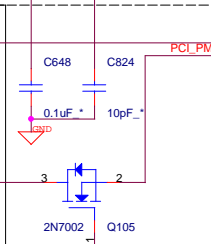
14,17 PCL\_REQ#1  
14,17,30,31 PCL\_PAR  
14,30,31 PCL\_C/BE#3  
14,30,31 PCL\_C/BE#2  
14,30,31 PCL\_C/BE#1  
14,30,31 PCL\_C/BE#0  
14 PCL\_GNT#1  
14,17,30,31 PCL\_FRAME#  
14,17,30,31 PCL\_IRDY#  
14,17,30,31 PCL\_TRDY#  
14,17,30,31 PCL\_DEVSEL#  
14,17,30,31 PCL\_STOP#  
14,17,30,31 PCL\_PERR#  
14,17,30,31 PCL\_SERR#  
25,30,38 PCL\_RSTNS#  
3,4,9,14,18,31,38 PCL\_RST#  
6,21 CLK\_CBPCI

#### CoreLogic CLOCKRUN#

15,17,22,25,31 PM\_CLKRUN#  
\*When do not use, please pull down it thru 100K.

#### Expansion Card PME / EC or CoreLogic GPI (WakeEvent)

\*It can be wire-or'd with other PCI devices since it have an open-drain driver.

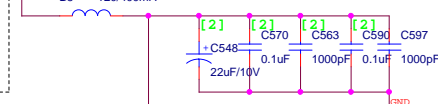


PCI AD31 P6  
PCI AD30 R6  
PCI AD29 T6  
PCI AD28 V6  
PCI AD27 W6  
PCI AD26 Z6  
PCI AD25 R7  
PCI AD24 T7  
PCI AD23 R8  
PCI AD22 T8  
PCI AD21 W8  
PCI AD20 W8  
PCI AD19 R9  
PCI AD18 T9  
PCI AD17 V9  
PCI AD16 W9  
PCI AD15 V12  
PCI AD14 W12  
PCI AD13 P13  
PCI AD12 R13  
PCI AD11 T13  
PCI AD10 V13  
PCI AD9 W13  
PCI AD8 R14  
PCI AD7 V14  
PCI AD6 W14  
PCI AD5 T15  
PCI AD4 V15  
PCI AD3 W15  
PCI AD2 V16  
PCI AD1 W16  
PCI AD0 V17  
R12  
R10  
T12  
T14  
W7  
W5  
V5  
T10  
V10  
W10  
R11  
DEVSEL#  
T11  
PERR#  
SERR#  
W11  
T2  
R5  
T5  
W4  
R1  
H9  
K9  
L9  
M9  
H10  
J10  
GND4  
GND5  
GND6  
GND7  
GND8  
GND9  
GND10

[1] NOT INSTALLED

[2] PLACE AS CLOSE AS POSSIBLE TO DEVICE TERMINALS

\*Layout as close as possible to AVCC\_PHY pins.



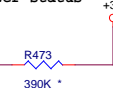
#### Caution! --- Making common planar with R5C476-II

\*Note that Ball A15,B15,B8,A8 (AVCC\_PHY for R5C552) are all connected to ground when mounting R5C476-II, since they are tied ground inside R5C576-II.

\*So, these balls should be left open when mounting R5C5476-II.

GUARD GND

Cable power status



\*Xtal  
\*Layout as close as possible to the chip. Surround by shield etch around this circuitry.

#### = Hardware Suspend input

\* If asserted, VCCPCI may be cut off.  
\* If do not use, it should be pulled high.

#### =>EC or CoreLogic RI/GPI (Ring Event)

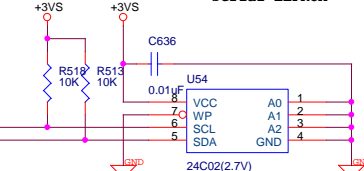
\*Unused TEST pin should be pull down thru a resistor. Do not connect to GND directly.

#### => Speaker Driver

\*SPKROUT# should be weakly pulled low externally when using EEPROM. Alternatively, pull up is required for no SROM activity.

( IRQ3-7 are GPIO when SERIRQ Mode )  
( SERIRQ, if Serial Interrupt mode )  
( IRQ10-11 are LEDA/B Output when SERIRQ mode. )

#### Serial EEPROM



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1394 Controller - R5C552

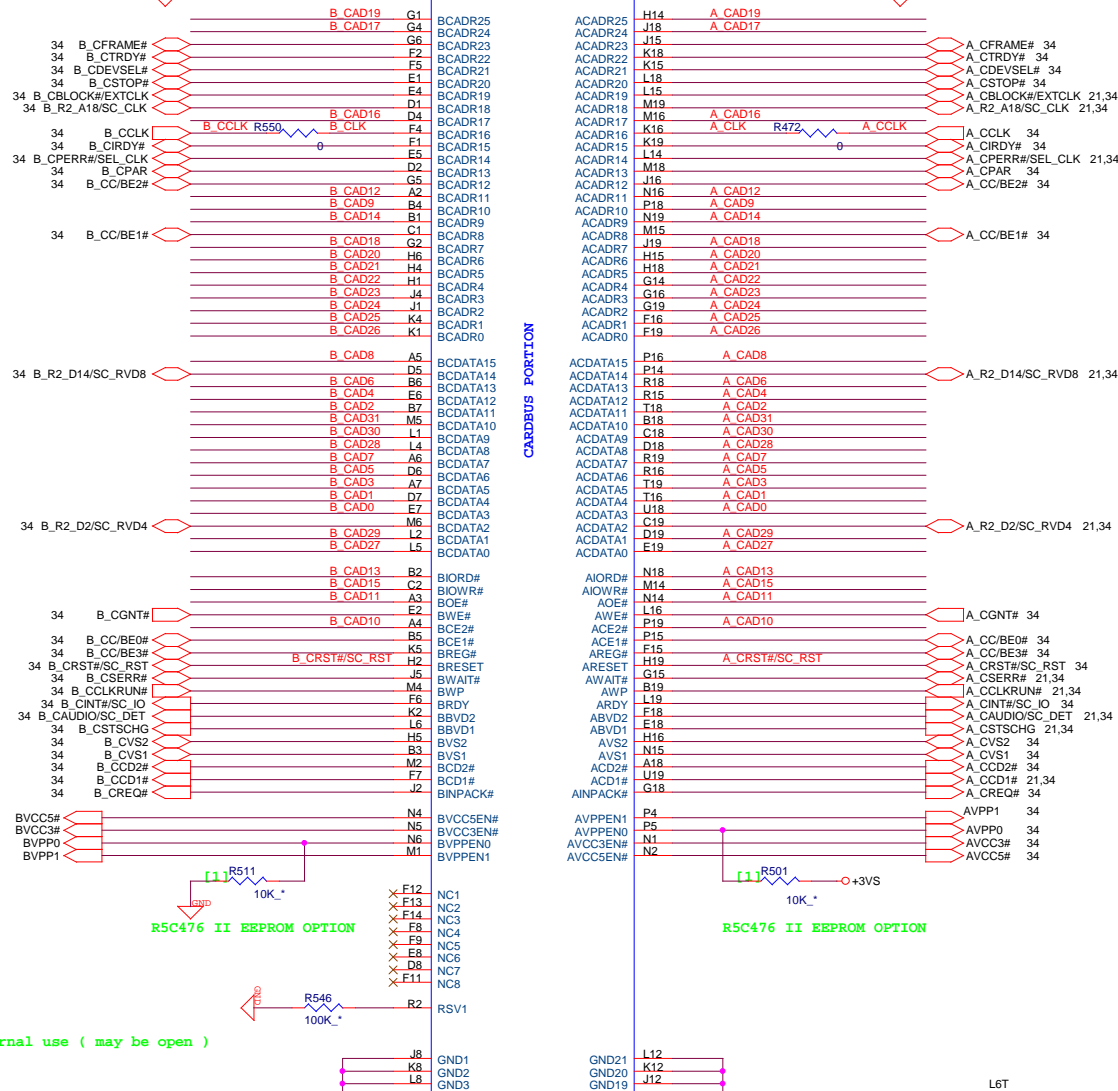
Size Custom

Document Number L3C

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A\_CAD[0..31] A\_CAD[0..31] 34  
B\_CAD[0..31] B\_CAD[0..31] 34



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Title

Cardbus Controller - R5C552

Size

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Date:

Tuesday, November 19, 2002

Sheet

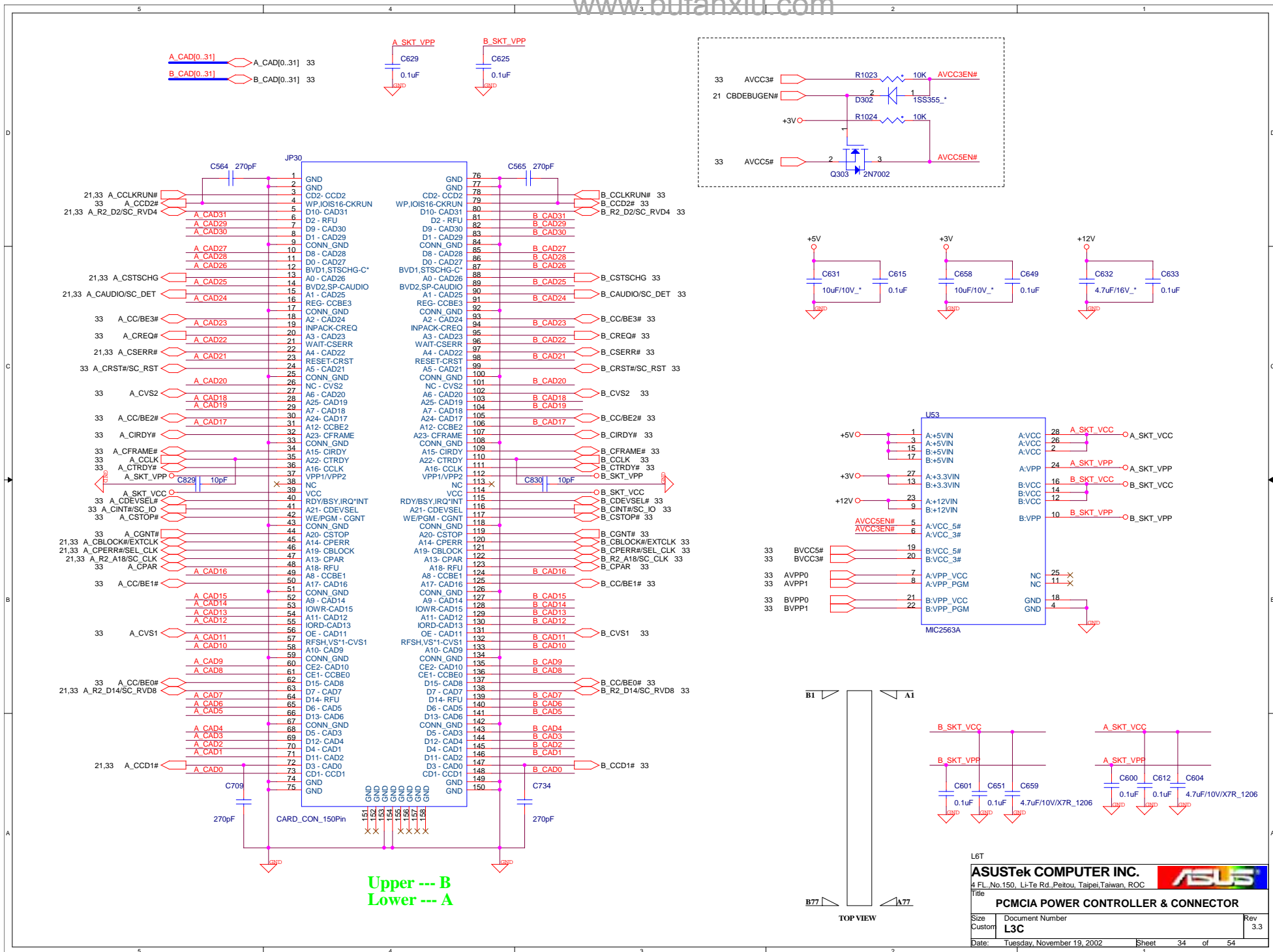
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PCMCIA POWER CONTROLLER &amp; CONNECTOR

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L3C

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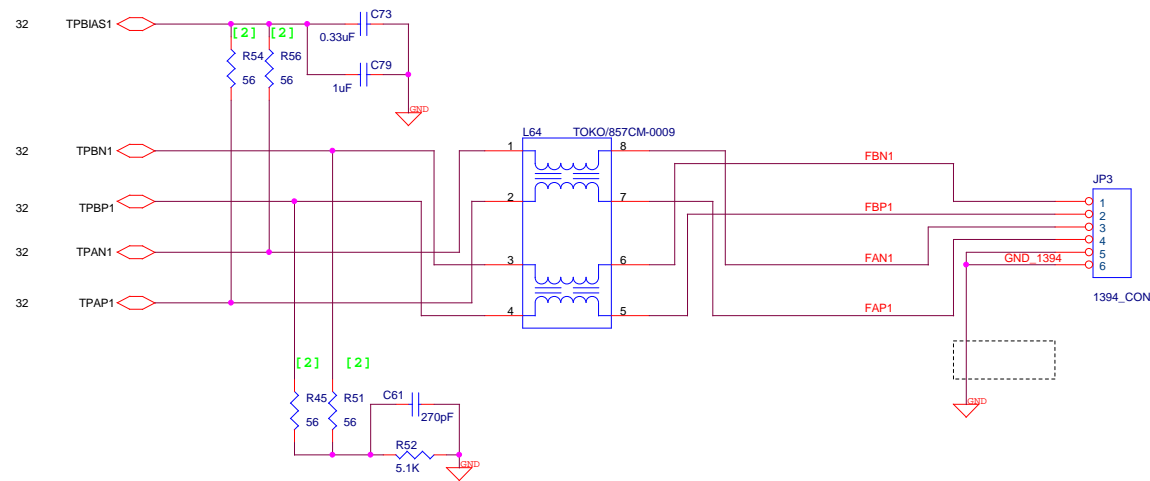
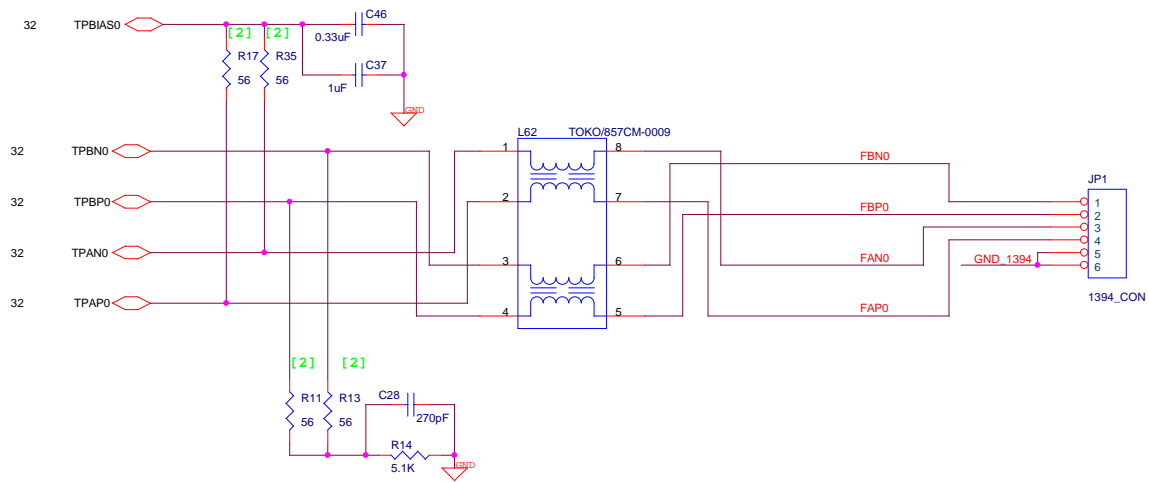
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\*TPA/TPA#,TPB/TPB# pair trace closely as possible  
 \*TPA/TPA#,TPB/TPB# pair trace must be the same length electrically  
 \*TPBIAS traces from pin to the filter capacitors short and wide.  
 \*Termination resistor for TPA+/- TPB+/- must be located as close as possible to its cable driver (device pin out).

- [1] NOT INSTALLED  
 [2] PLACE AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.  
 [3] SOLDER MASK.

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Title

1394 Port

Size

Document Number

L3C

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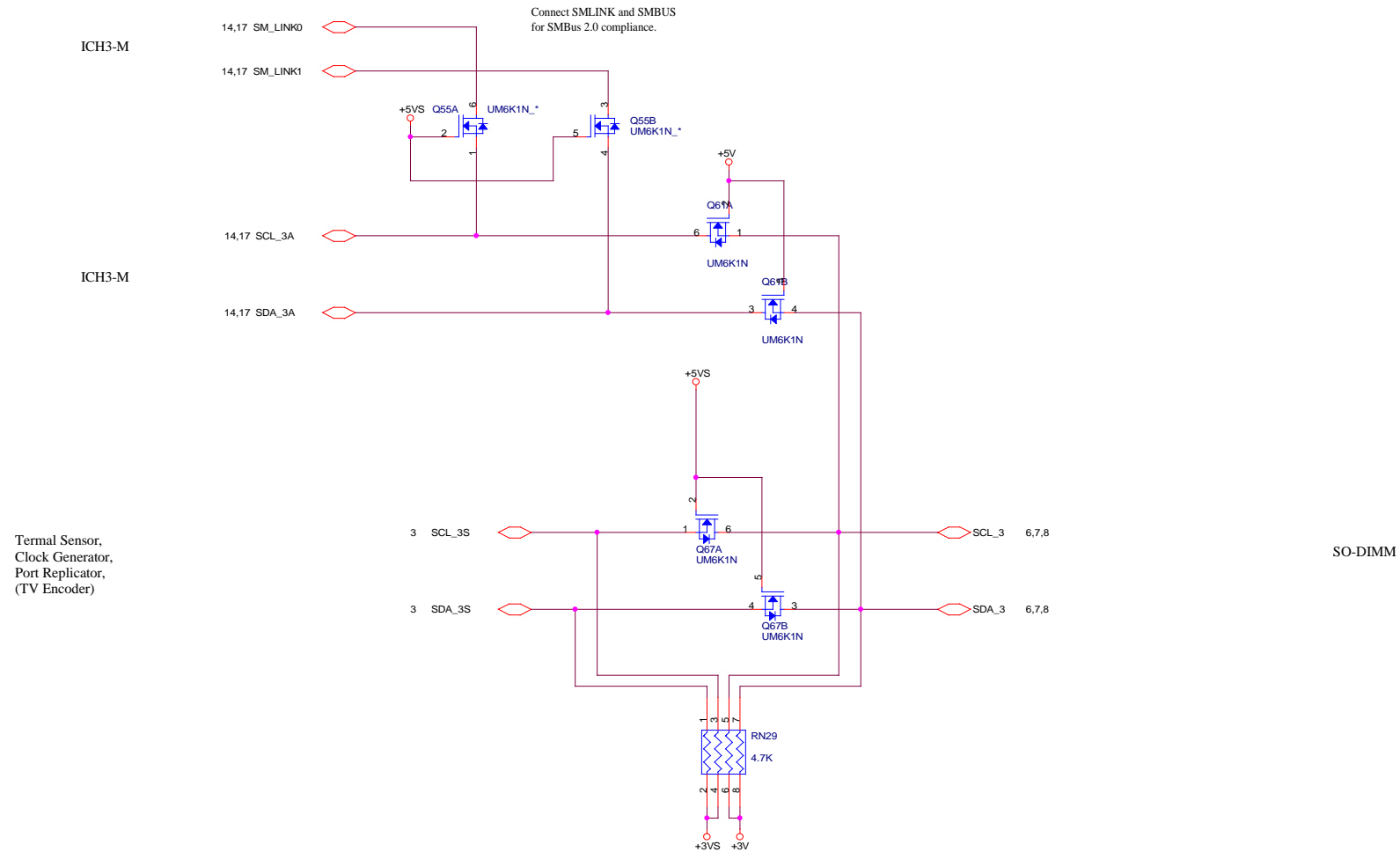
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Title

SM BUS

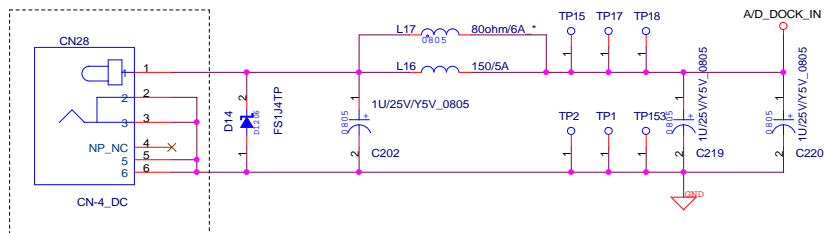
Size  
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L3C

Rev  
3.3

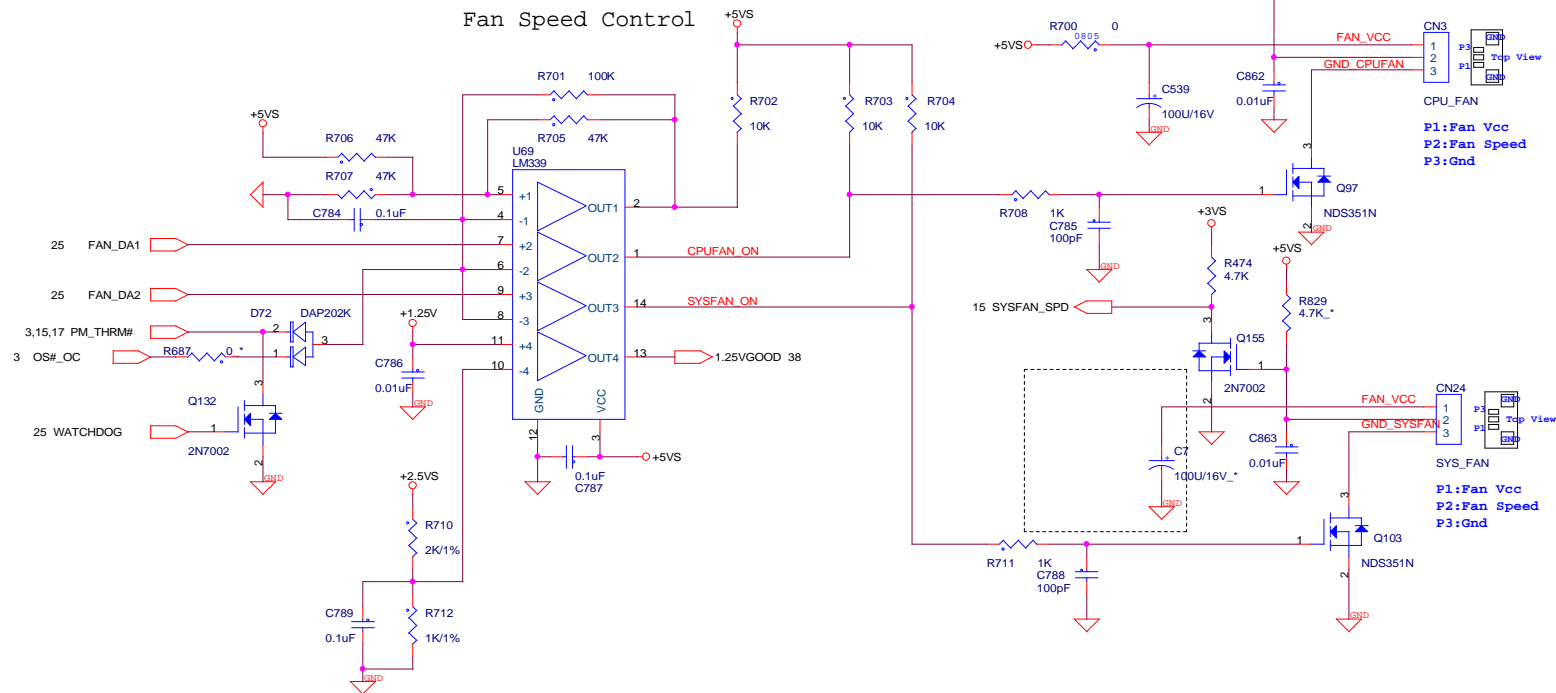
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Add Metal Shielding  
on DC-IN Jack

### Fan Speed Control



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Title

FAN &amp; AC-IN

Size

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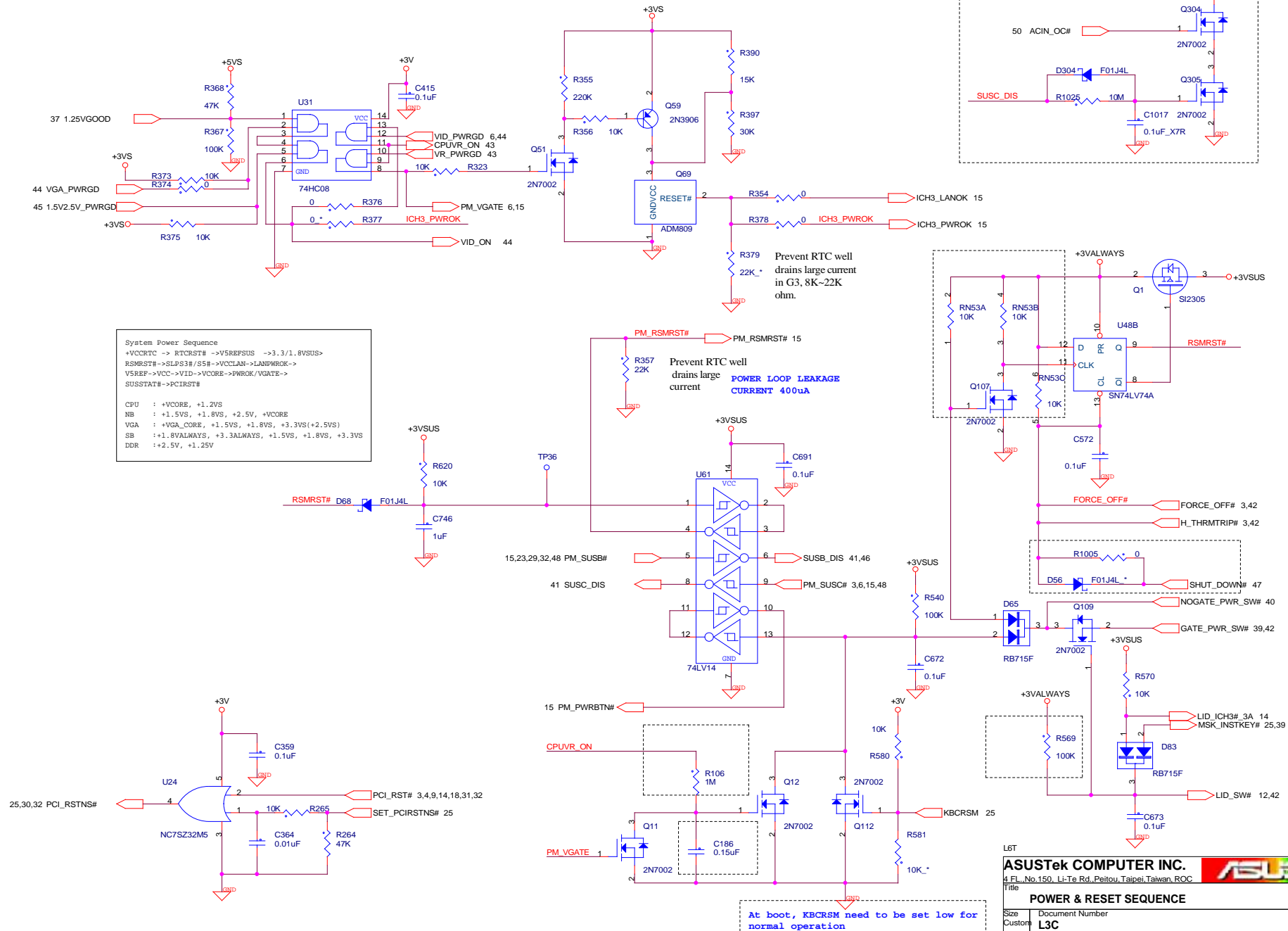
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Rev

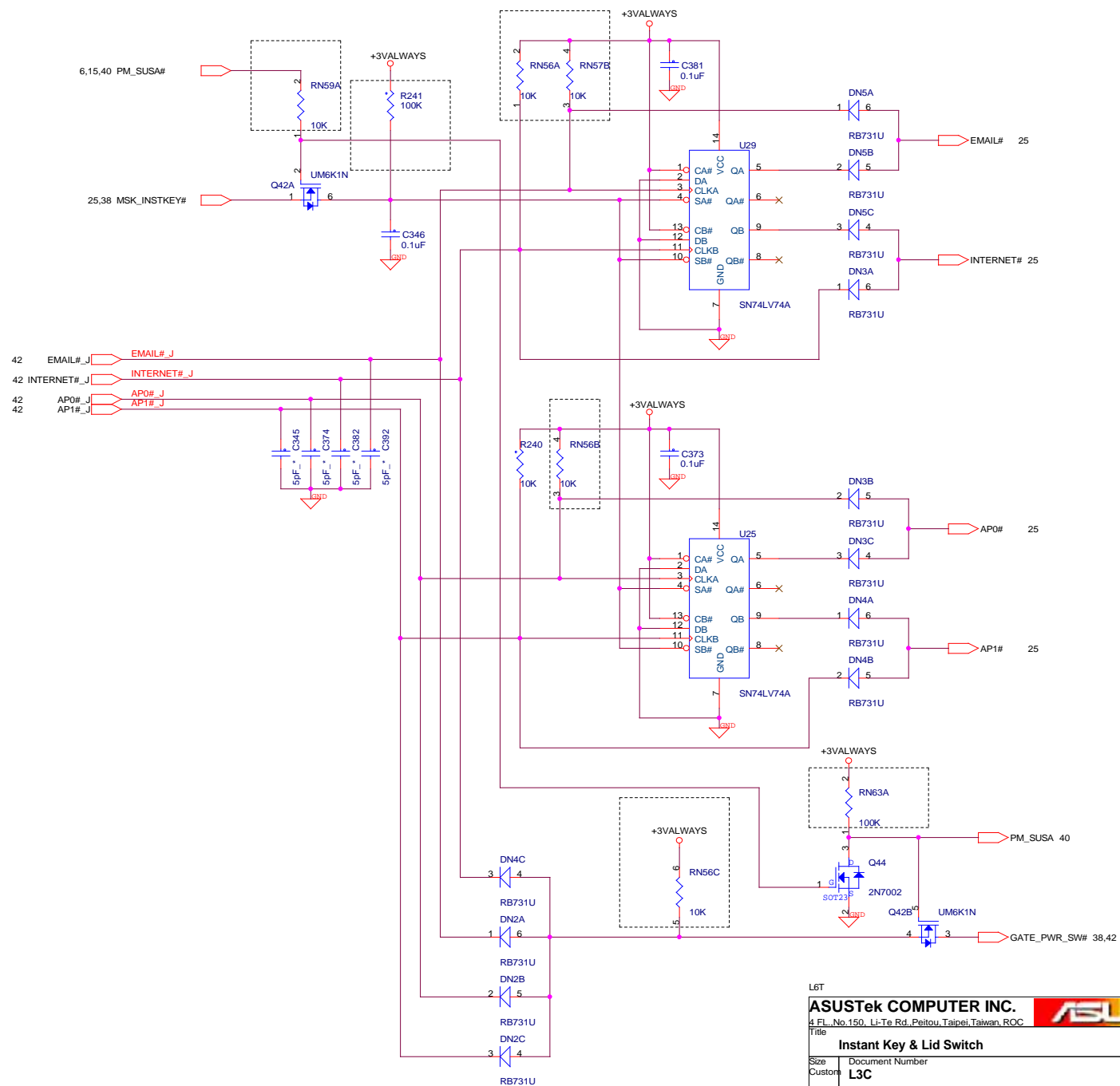
3.3

System Power Sequence  
 +VCCRTC -> RTCRST# -> +V5REFSUS -> 3.3/1.8VSUS  
 RSMRST# -> SLP/S5# -> VCCLAN -> LANPWROK ->  
 V5REF -> VCC -> VID -> VCORE -> PWROK/VGATE ->  
 SUSSTAT# -> PCIRST#

CPU : +VCCORE, +1.2VS  
 NB : +1.5VS, +1.8VS, +2.5V, +VCCORE  
 VGA : +VGA\_CORE, +1.5VS, +1.8VS, +3.3VS(+2.5VS)  
 SB : +1.8VALWAYS, +3.3ALWAYS, +1.5VS, +1.8VS, +3.3VS  
 DDR : +2.5V, +1.25V



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Title		
<b>POWER &amp; RESET SEQUENCE</b>		
Size	Document Number	Rev
Custom	<b>L3C</b>	3.3
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Title

Instant Key &amp; Lid Switch

Size

Document Number

Custom

L3C

Date:

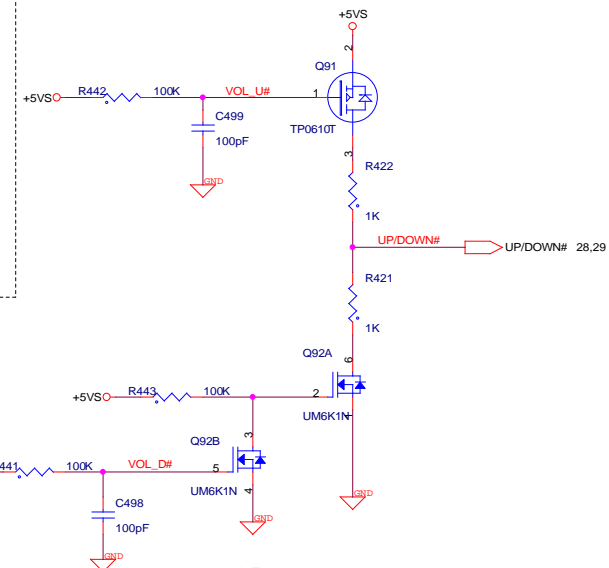
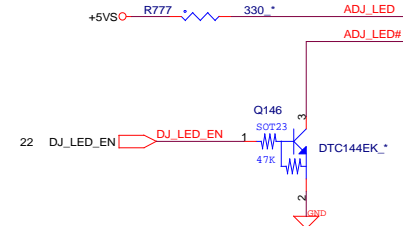
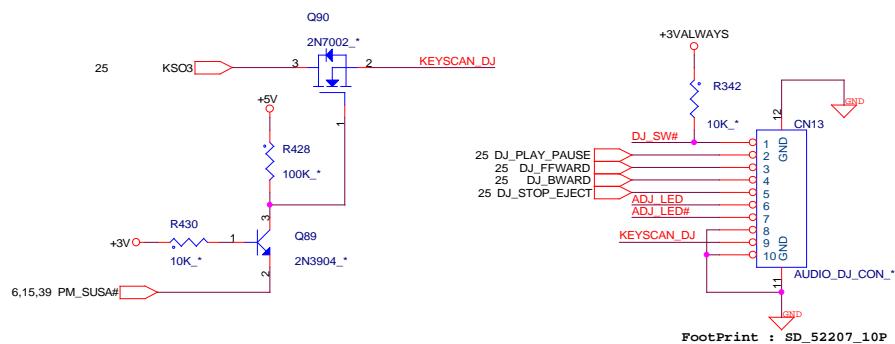
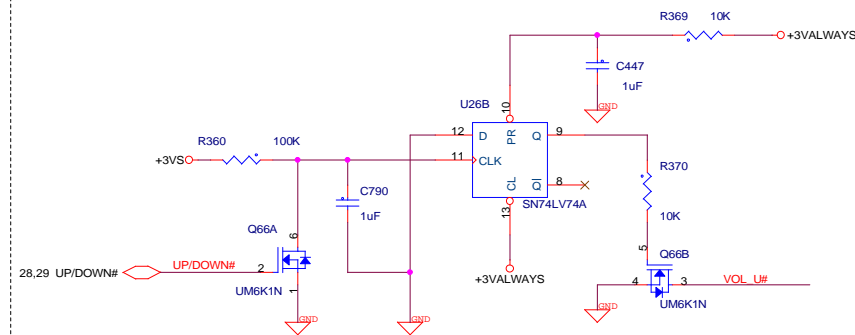
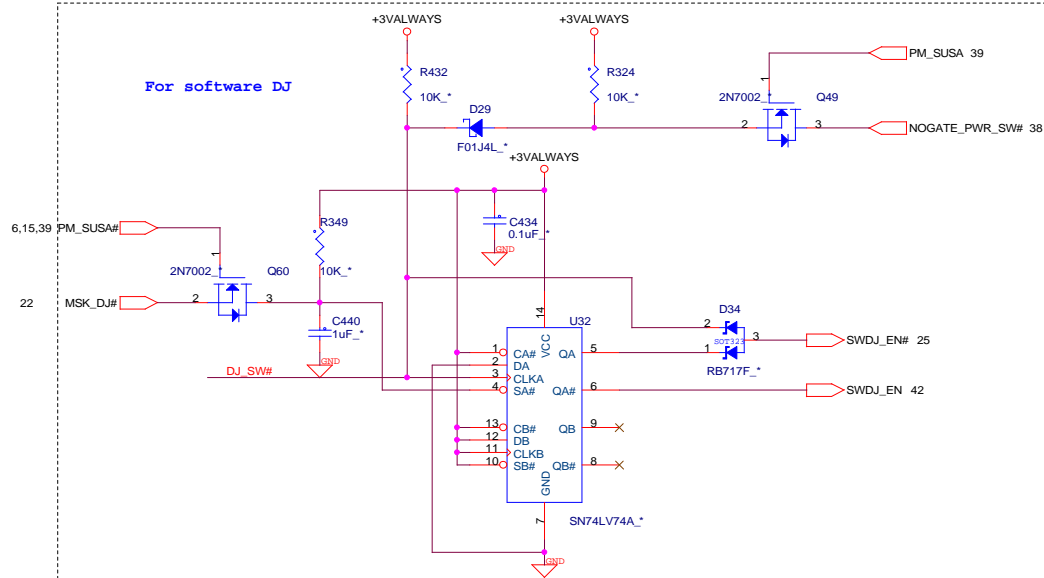
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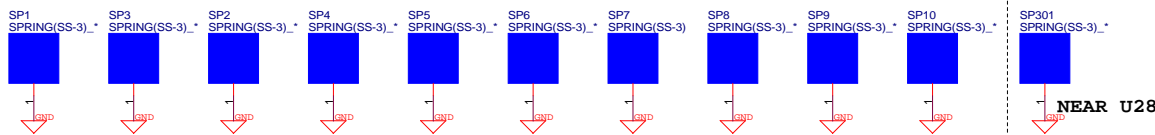
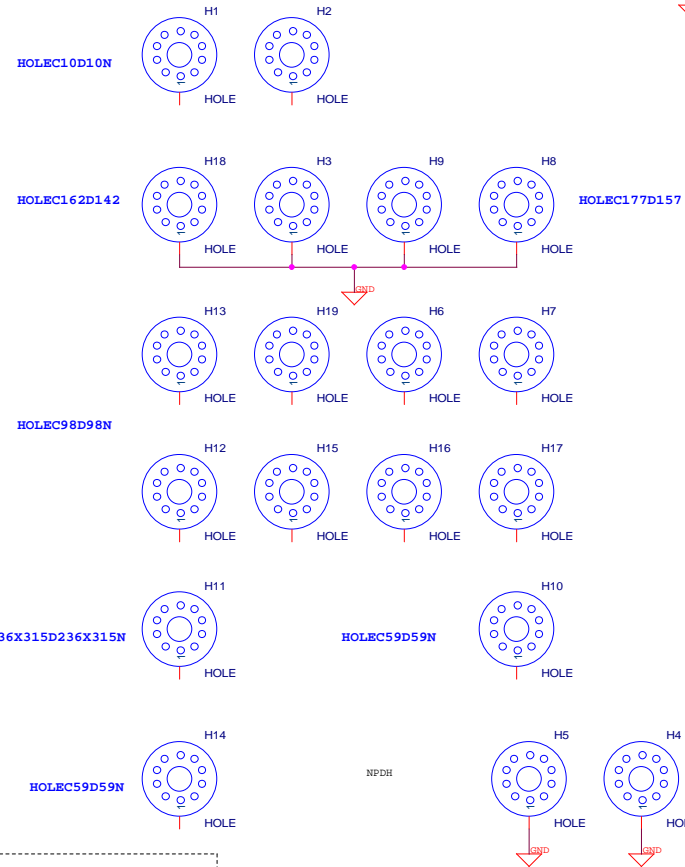
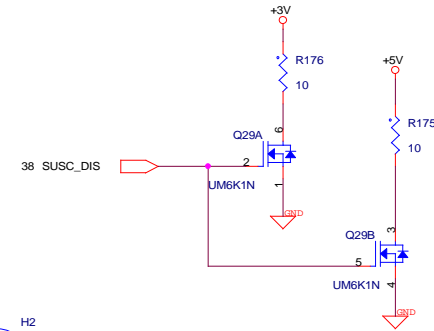
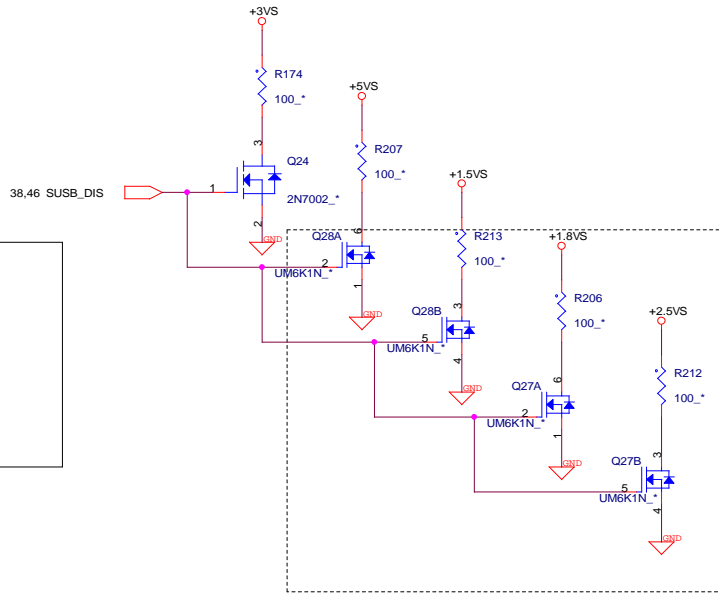
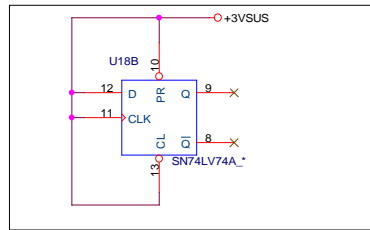
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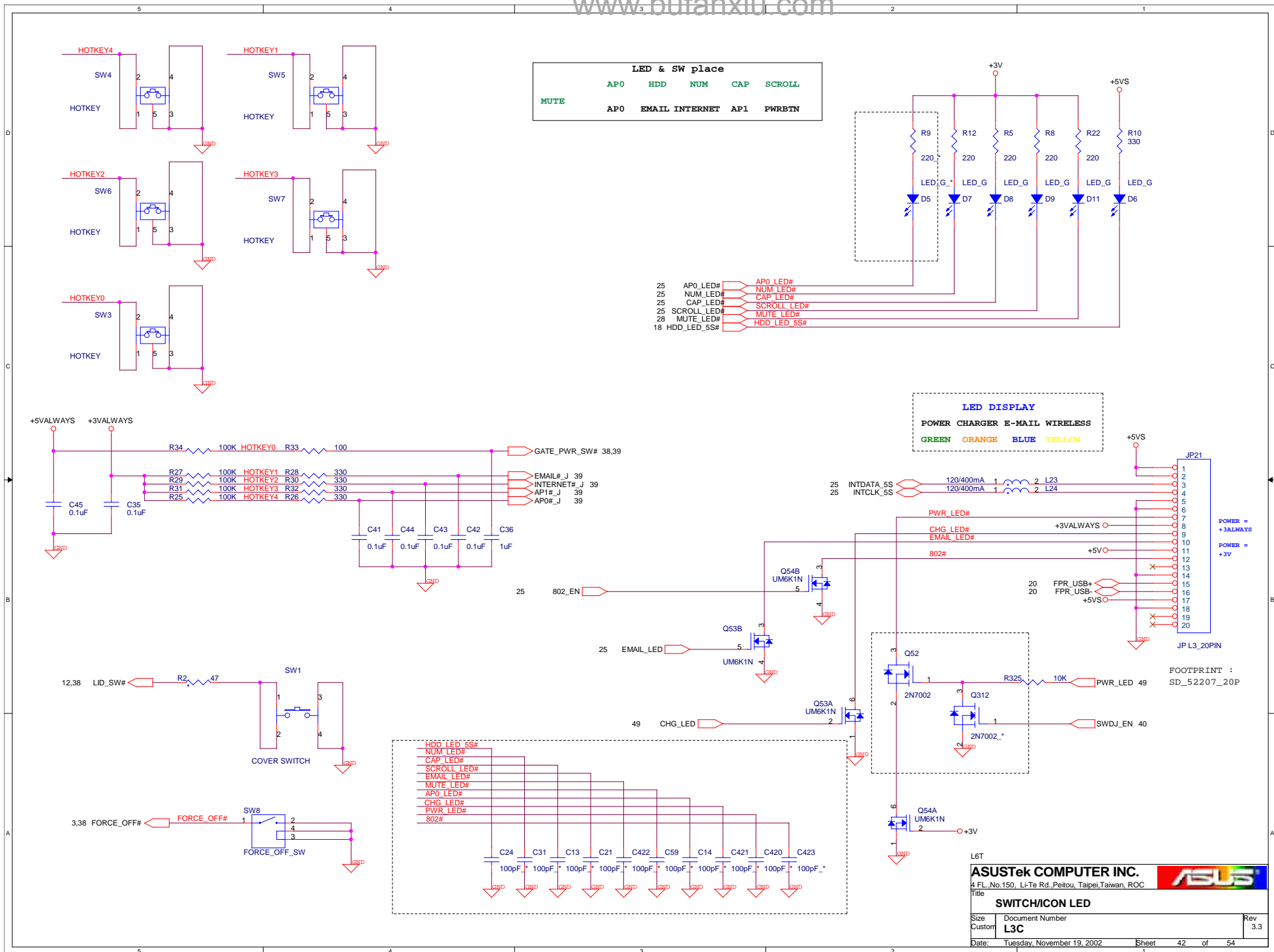
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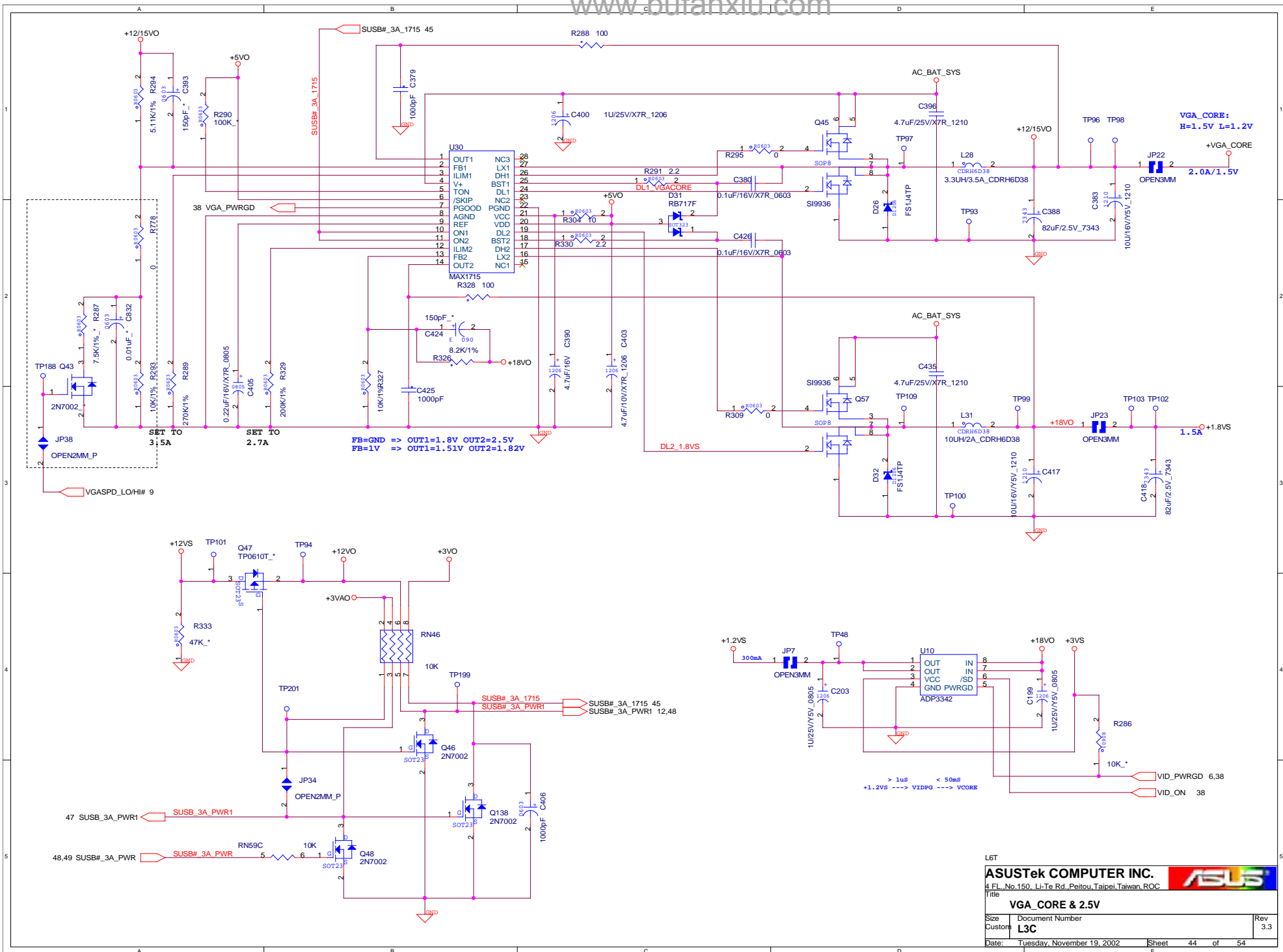
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4 FL, No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC		Title	
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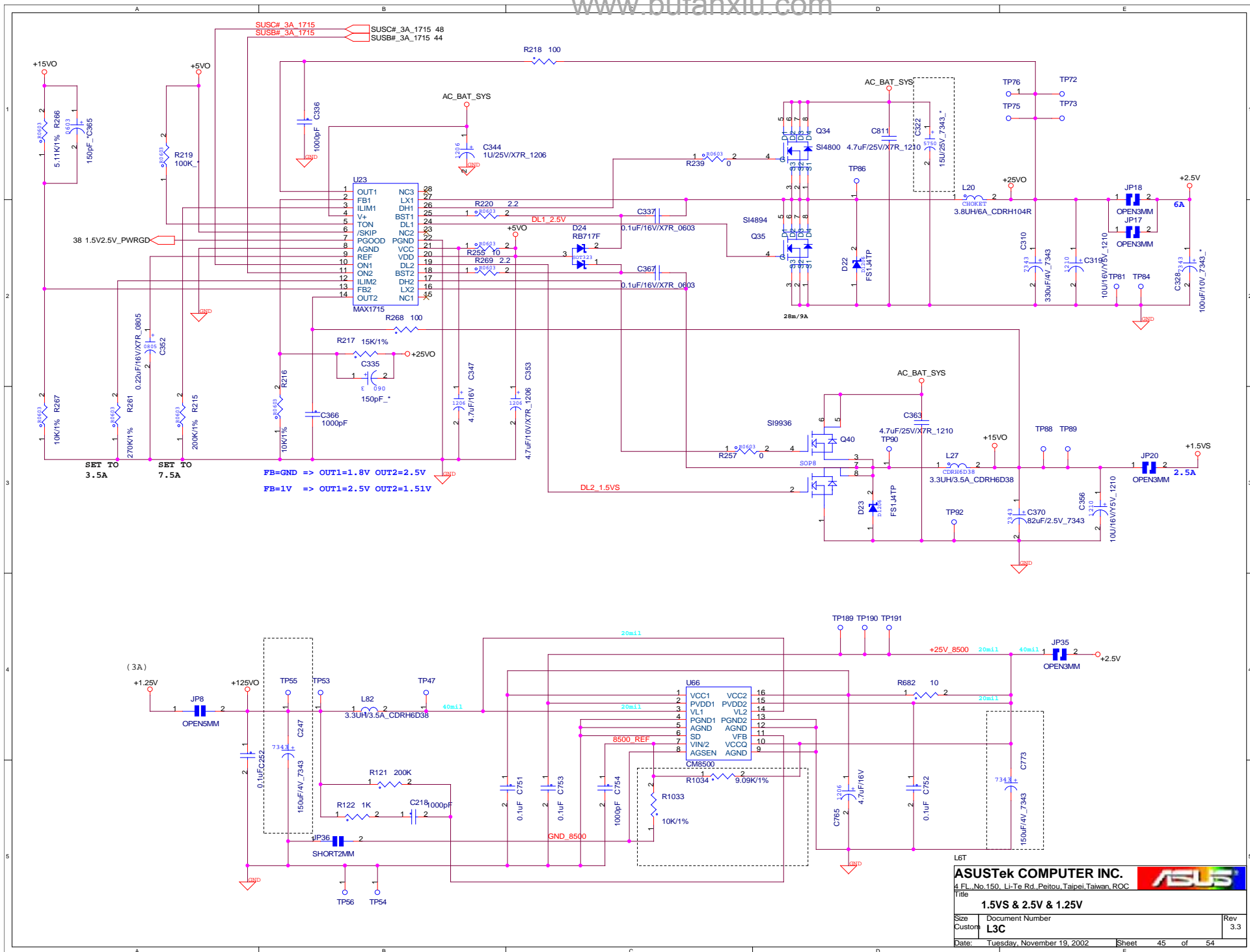


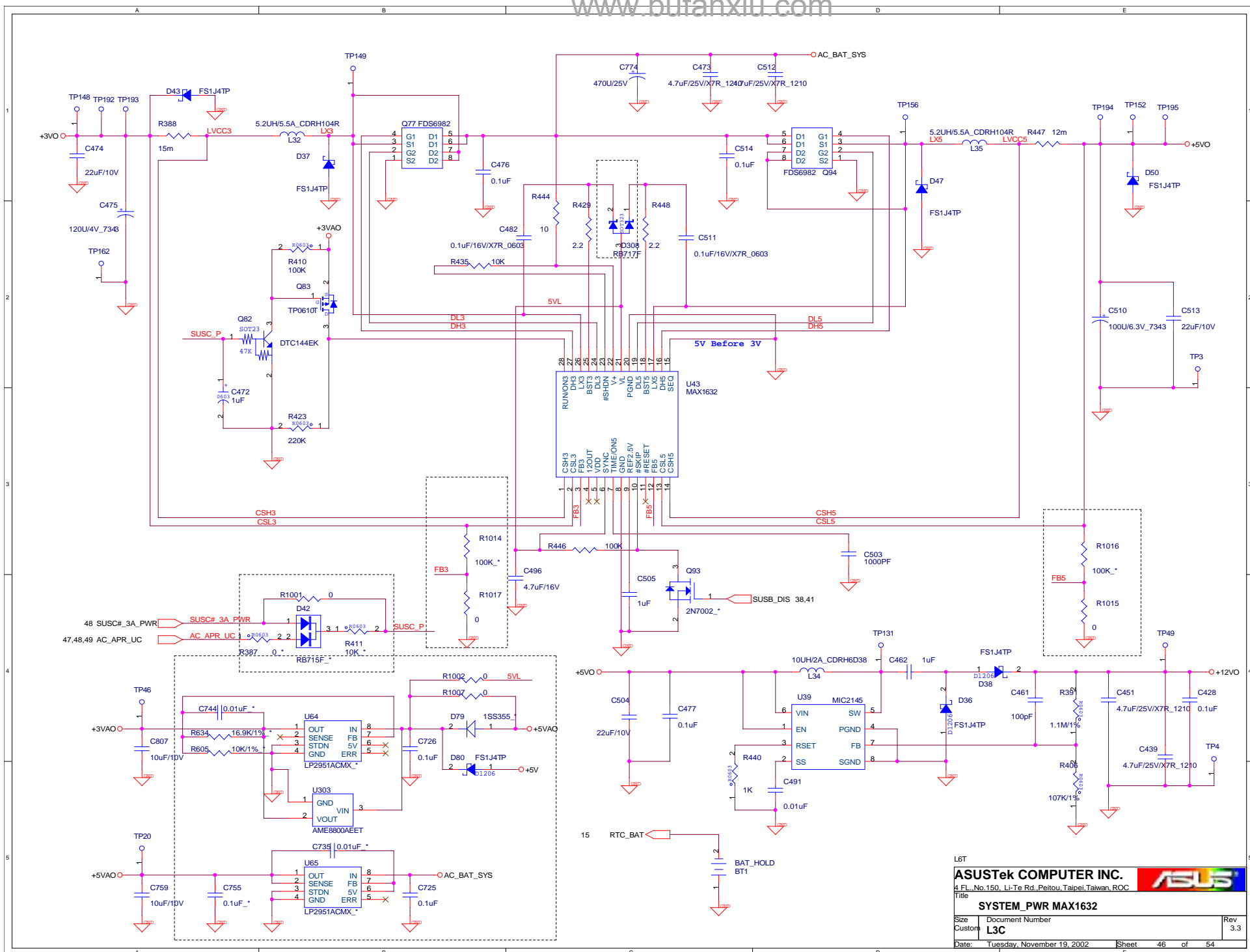
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**SYSTEM\_PWR MAX1632**

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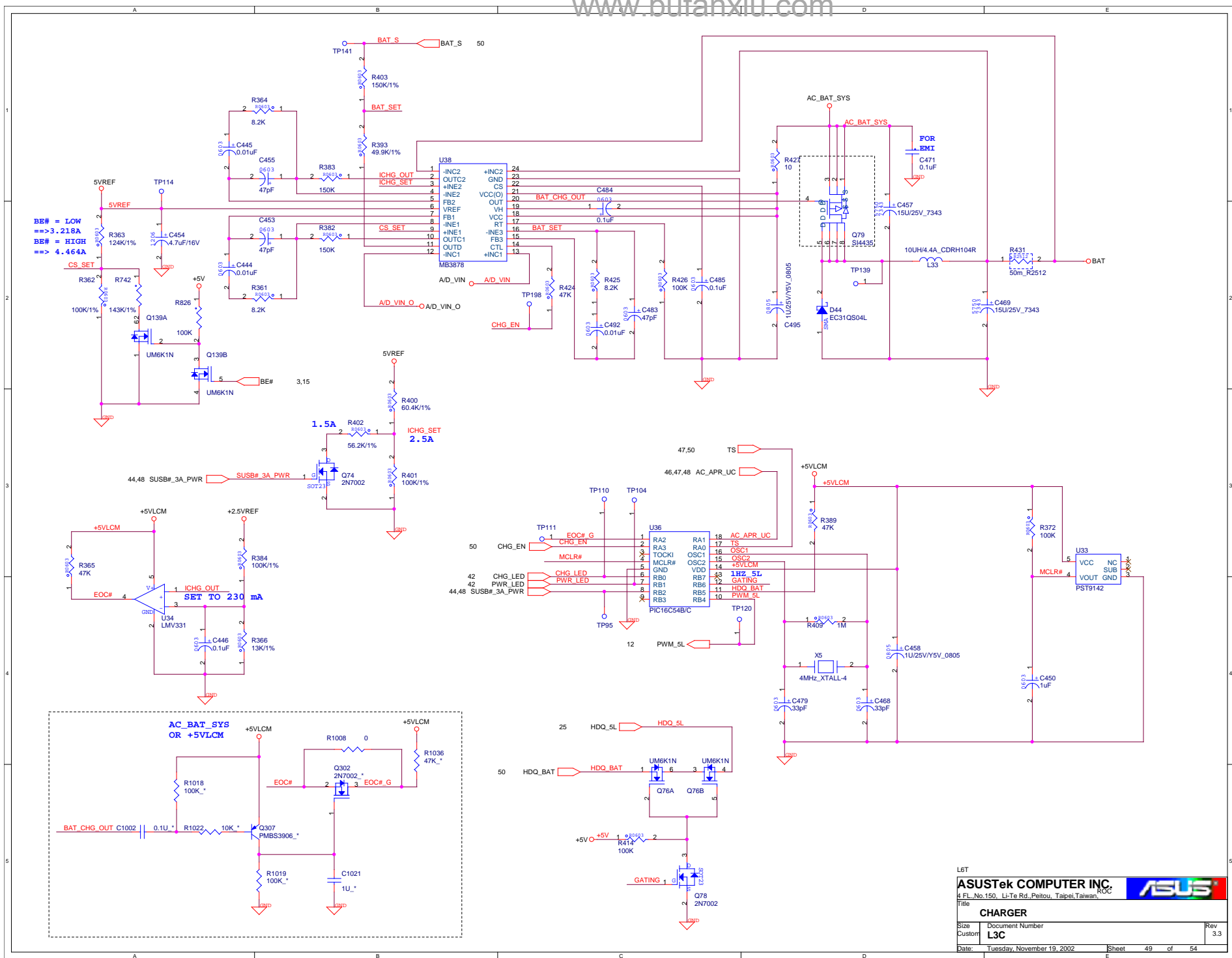
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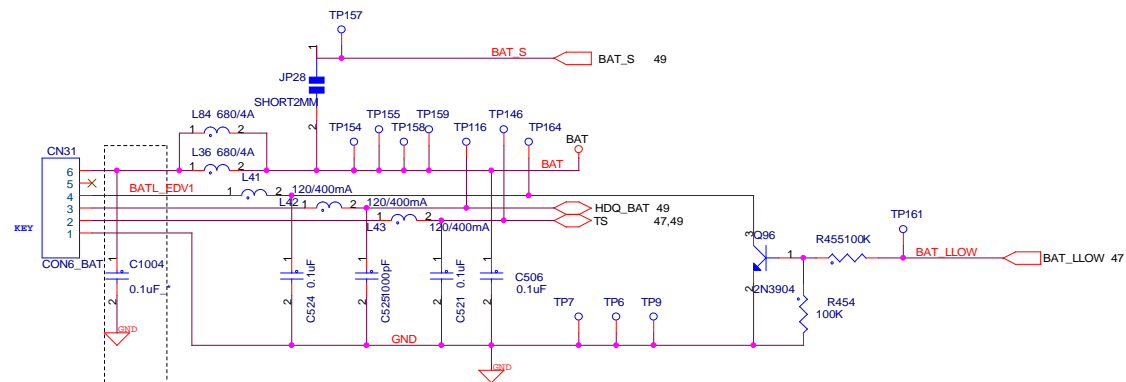
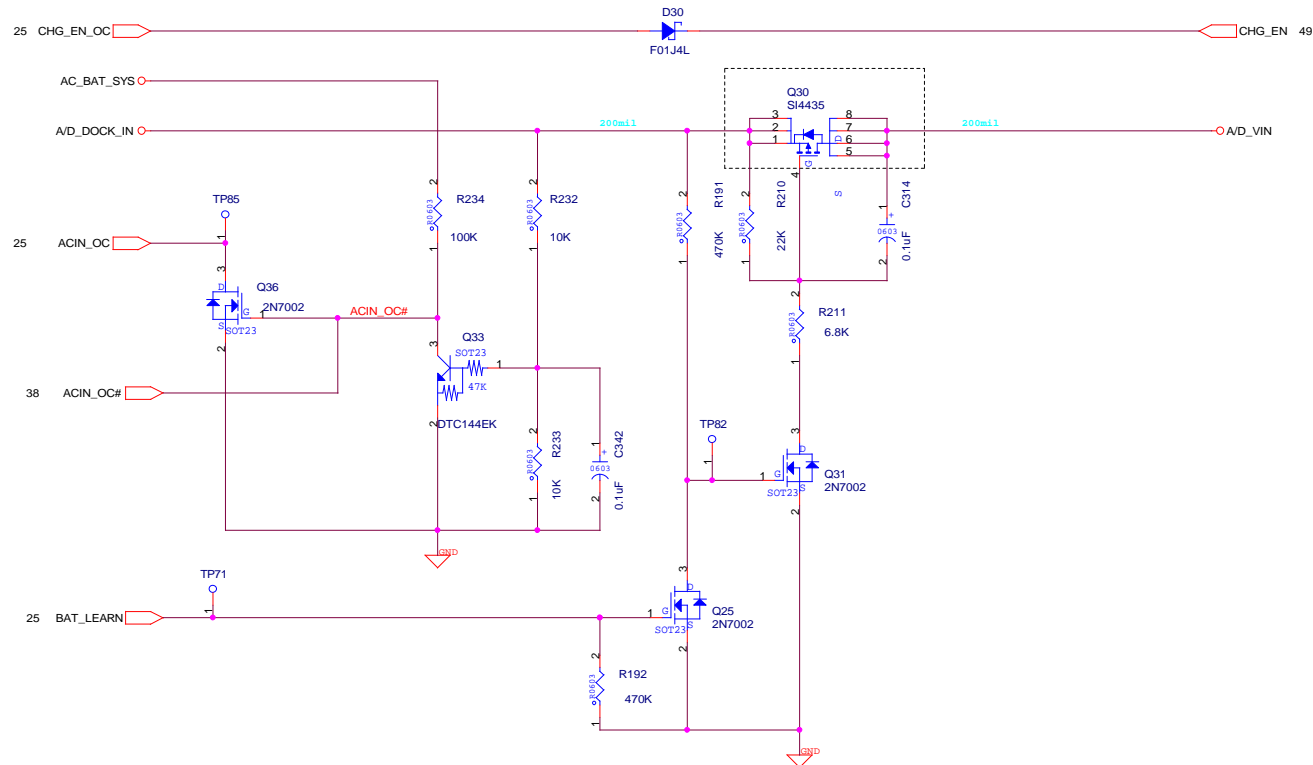
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CHARGER

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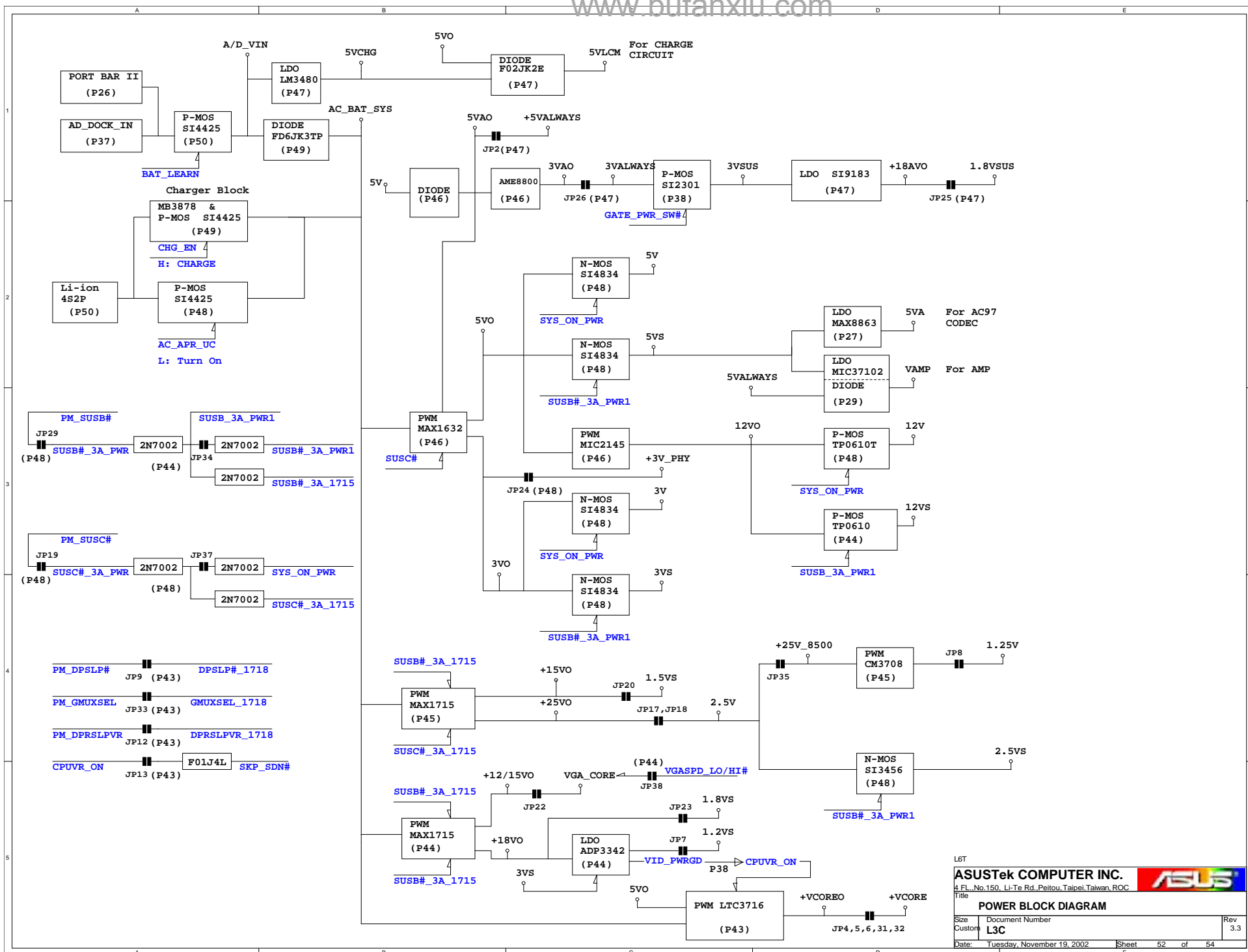
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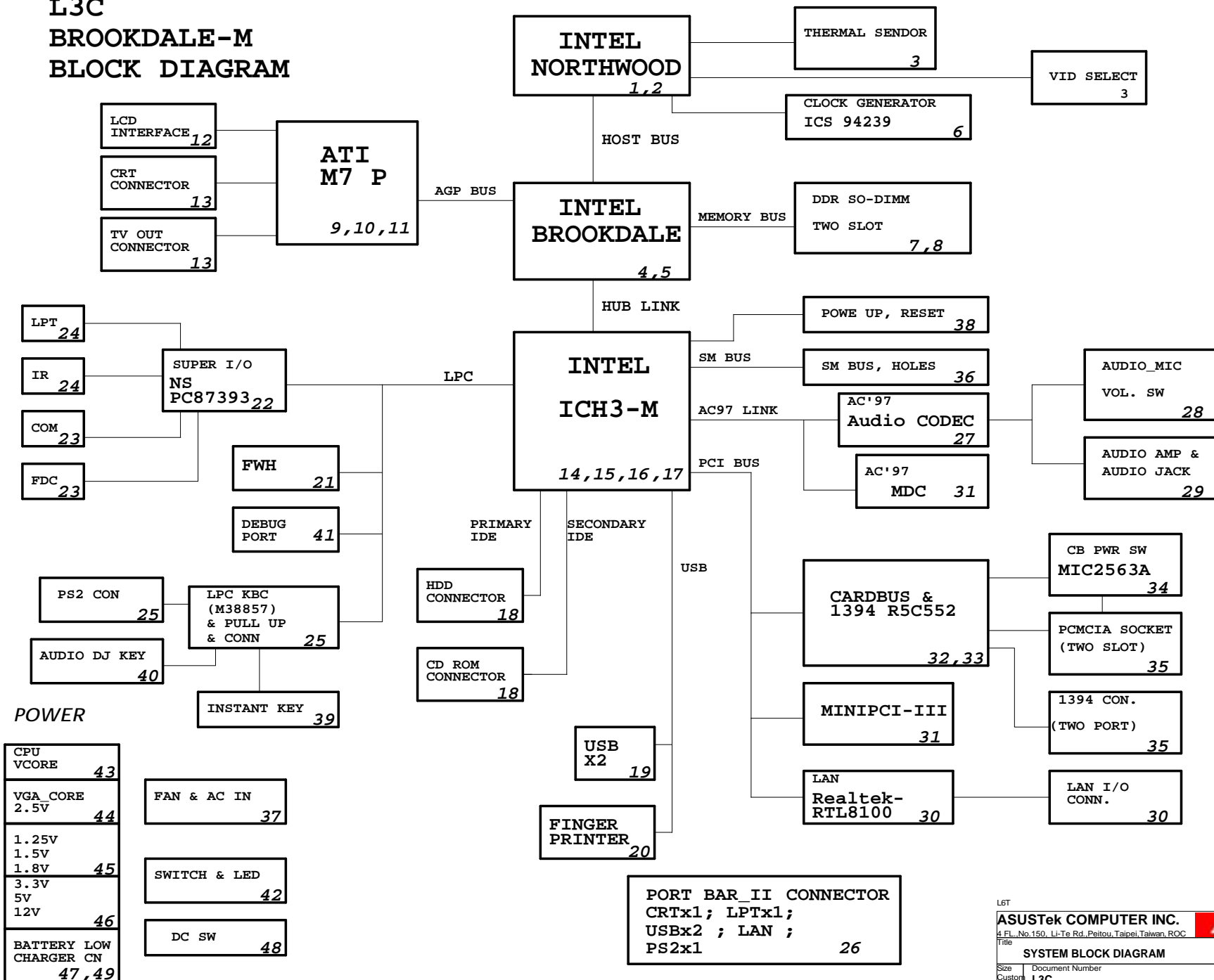
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# L3C BROOKDALE-M BLOCK DIAGRAM



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P.1--CPU NORTHWOOD - 1  
 P.2--CPU NORTHWOOD - 2  
 P.3--HERMAL & HW MON  
 P.4--NB BROOKDALE - 1  
 P.5--NB BROOKDALE - 2  
 P.6--CLOCK ICS94239  
 P.7--DDR SODIMM - 1  
 P.8--DDR SODIMM - 2  
 P.9--ATI M7-D - 1  
 P.10--ATI M7-D - 2  
 P.11--ATI M7-D - 3  
 P.12--LVDS & BACKLIGHT  
 P.13--TV & CRT  
 P.14--ICH3 - M - I/F 1  
 P.15--ICH3 - M - I/F 2  
 P.16--ICH3 - M - DECOUPLING  
 P.17--ICH3 - M - PULLUP  
 P.18--IDE & CD-ROM  
 P.19--USBx2  
 P.20--Finger Print \_OP  
 P.21--FWH  
 P.22--SUPER I/O 87393  
 P.23--FDD & COM1  
 P.24--IR & LPT  
 P.25--KBC & PS2  
 P.26--PORT BAR II  
 P.27--AC97 & MDC  
 P.28--MIC , VOL SW  
 P.29--AUDIO AMP.  
 P.30--LAN-RT8100L  
 P.31--MiniPCI  
 P.32--R5C552/1394OHCI  
 P.33--R5C552/CARDBUS  
 P.34--PCMCIA PWR(2563A) & CON  
 P.35--PHY CONNECTORS ( 2PORT )  
 P.36--SM BUS  
 P.37--FAN & AC-IN  
 P.38--PWR & RESET\_SEQ  
 P.39--INSTANT KEY  
 P.40--Audio DJ - KEY  
 P.41--DISCHARGE, DEBUG PORT, HOLE  
 P.42--SWITCH,ICON LED  
 P.43--VCORE INTERSIL 6215  
 P.44--VGA\_CORE & 1.8V  
 P.45--1.5VS & 2.5V & 1.25V  
 P.46--SYSTEM POWER MAX1632  
 P.47--BATLOW  
 P.48--DC SWITCH  
 P.49--CHARGE  
 P.50--BAT LEARNING  
 P.51--VGA-MEM

**Resource Assignments**

LAN : AD21(DEV. A), PCI\_REQ#0, PCI\_INTD#  
 CARDBUS 1394: AD23(DEV. C), PCI\_REQ#1, PCI\_INTA#, PCI\_INTB#,PCI\_INTC#  
 MINIPCI : AD24(DEV. D), PCI\_REQ#3, PCI\_INTC#, PCI\_INTD#  
 VGA : PCI\_INTA#  
 AC97 : PCI\_INTB#  
 USB 0,1 : PCI\_INTA#  
 USB 2,3 : PCI\_INTD#  
 USB 4,5 : PCI\_INTC#

SMBUS (ICH3) : HW Monitor,CLK,Inverter ( Pull up = +3VS )  
 (PullUp= +3VSUS) DDR\_SODIMM ( Pull up = +3V )


SMBUS ADDRESS : CLK = 1101001x ( D2 )  
 HW Monitor (CPUT1) = 1001001 (Default)  
 HW Monitor (CPUT2) = 1001000 (Default)  
 HW Monitor (OTHER) = 0101101x (Default)  
 DDR\_SODIMM1 = 000  
 DDR\_SODIMM2 = 001  
 INVERTER = 0101000x

DQ BUS : M38859 , PIC16C54 , BQ2050 (BATTERY)

	S1	S3	S4	S5
RTCVCC	ON	ON	ON	ON
+5VALWAYS	ON	ON	ON	ON
+3VALWAYS	ON	ON	ON	ON
+3VSUS	ON	ON	ON	ON
+1.8VSUS	ON	ON	ON	ON
+12V	ON	ON	OFF	OFF
+5V	ON	ON	OFF	OFF
+3V	ON	ON	OFF	OFF
+2.5V	ON	ON	OFF	OFF
+1.25V	ON	ON	OFF	OFF
+VCORE	ON	OFF	OFF	OFF
+1.2VS	ON	OFF	OFF	OFF
+5VS	ON	OFF	OFF	OFF
+3VS	ON	OFF	OFF	OFF
+2VS	ON	OFF	OFF	OFF
+2.5VS	ON	OFF	OFF	OFF
+VGA_CORE	ON	OFF	OFF	OFF
+1.5VS	ON	OFF	OFF	OFF
+1.8VS	ON	OFF	OFF	OFF
CLOCK	ON	OFF	OFF	OFF

P.52--POWER BLOCK DIAGRAM  
 P.53--SYSTEM BLOCK DIAGRAM  
 P.54--FILE LIST

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